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Wireless Sensor Network of 3 – Bit ADC

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Abstract:- More recent attention is focused on smart dust or on wireless sensor networks. Sensor and process-type, autonomous, very low-powered electronic devices transmit data from one node (mote) to another in an ad-hoc network by transmitting the environment variations. The smart dust subsystems generally include analog (AI) interface, analog-to-digital (ADC), digital signal processor (DSP), digital-to-analog (DAC), and power management and communication transceiver. A clock less EDADC system is presented using the technique of CT delta modulation (DM). The ADC output is digital, time-controlled, data token. The ADC uses a DAC feedback, which is area efficient and segmented resistor string. There is a study of various R-string DAC architectures. A comparison of a component reduction to a prior art indicates that the DAC and D flip-flops in 8-bit ADC bidirectional register have reduced resistors and switches by nearly 87.5 percent using the proposed segmented DAC architecture. SNDR is 22.696 dB, 30,435 dB and 55.73 dB respectively, for the 3-bit, 4-bit and 8-bit systems, and interest ranges are as high as 220.5 kHz.

Keywords:- *Event-Driven (ED), Continuous Time (CT), Delta-Modulation (DM), Digital Signal Processing (DSP).*

I. INTRODUCTION

The aim of this paper is to study and design a mixed signal processing system consisting of a smart dust application in a test-driven method, consisting of a digital signal processor (DSP) and analog to digital conversion device (ADC), digital to analog converter (DAC). The entire system must be operated without sampling in CT mode. The most point is to realize less vitality utilization and range without relinquishing system performs generally. In the last few years, there has been a phenomenon known as "intelligence dust," also known as "motes." Smart dust is a minute, high power electronic sensor independent device, packaged with different sensors, intelligence, and even remote communication capabilities (density of a sand-particle and size).

The smart dust motes used as an ad-hoc network, known as remote sensor, may be a typical scenario for sensing the variables of the environment such as pressures, heat, illumination, oscillation, magnetic induction or biophysical chemistry.

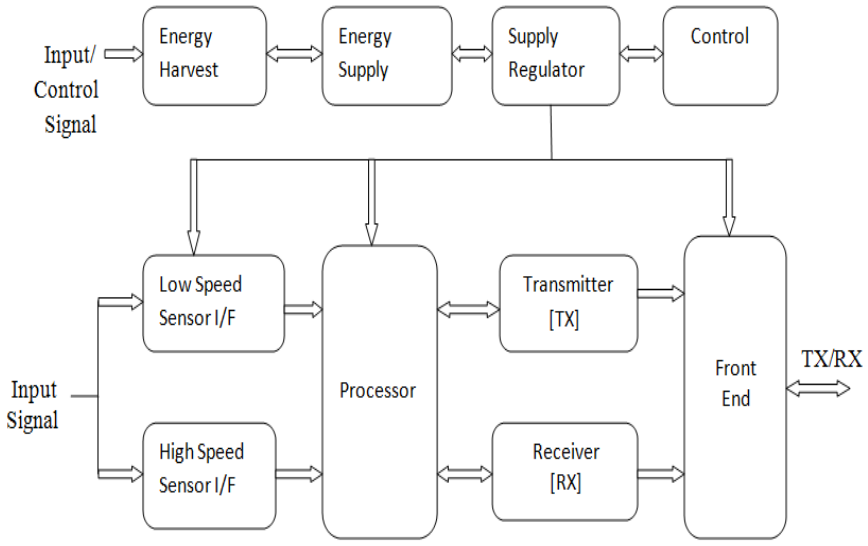

Fig 1:- A typical Smart Dust Mote Block Diagram

This network collected and processed data from one mote to another [1]. Intelligent dust can be derived either from the batteries or the environment itself, or from both. The details of the block level of one stand-alone a commonplace mots module comprises of a vitality collector, vitality capacity, supply controller, high-speed sensor and low-speed sensor interface, DSP and radio handset segment. Fig.1.energy harvest using an energy

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storage element, the control circuit is capable to different control components include in swarming operation and sensors collect and convert environmental changes into an analog electric signal equivalent. The data is proceeding with a DSP. Essentially, operation in digital system can perform different types of physical system operations, such as filtering, domain transformation, compression, encryption, etc.

Smart dust is investigates the limitations of micro fabrication technology to determine whether an autonomous sensing, computing and communication system. It is used to reduce the cost and size [1]. Digital processing quantized signals produce no aliasing and reduce the in-band quantization error [2]. Event driven analog to digital conversion and associated digital signal processing techniques are reviewed. Such techniques are still in research stage such as consumption of energy and band width resource[3,7]. We have presented a chip that converts analog signal to digital domain. Our result indicates that continuous time digital signal processing with certain properties [4]. An Event-Driven 8-bit ADC with a Segmented Resistor-String DAC is discussed in [5]. Clock less Asynchronous Delta Modulator Based ADC for Smart Dust Applications are shown in [6]. Analysis and simulation of continuous-time digital signal processorsare expained [8]. Energy-efficient serial modified element with large controllability explained [9]. GHz-range continuous-timeprogrammabledigitalFIRwithpowerdissipationthatauto maticallyadaptstosignalactivity is explained in [10].Mixed-Domain Systems and Signal Processing Based on Input Decomposition are shown in [11]. To avoiding aliasing effect and reducing quantization error in continuous time signals processor are discussed in [12]. A Low Power Tunable Delay Element Suitable for Asynchronous Delays of Burst Information is explained in [13]. Analysis and implementation of Continuous-time digital signal processors is explained in [14].

II. SMART DUST

Table 1 show the CTDSP system specifications, which will finally be implemented in the smart dust motes. Sea pressure imposed on that system is a clock lessens of all the blocks of the design. In addition, the complementary metal-oxide semi conductive (CMOS) process it is necessary implemented in 92 nm increased. ADC, DAC and FIR (Finite-Impulse-Response) Low Pass Filters (LPF) transverse direct form specifications are shown in Table 1. The handling is carried out in not continuous time, as opposed to conventional sampled systems. To operate signal processed in digital continuous time as sensed data from analog sensor module. connecting block and produces the RF output at the front end because input data are bursting and appear occasionally, where CTDSP system is very beneficial to remain idle almost of time and only work when important data are required for processing. A standard DSP system operates with a global clock signal or reference. At the rising or falling edge related to clk signal, and input message x (t) is sampling and quantified for pointing system triggered. The digital signal is reconstructed in analog equivalent by the DAC output. Entire system is fully synchronized through global clock. Disadvantages of conventional DSP systems are such a sampled arrangement requires a large fan-out clock, as many transistor doors have to be powered. The frequency of sampling is therefore determined for basis of highest frequency component of the input signal, making it expensive to execute both in terms of area and energy consumption.

Item	Parameter	Min	Type	Max	Unit
ADC	Resolution	5	3	9	bits
	Maximum input signal frequency	—	19	—	kHz
LPF	Sampling frequency	—	45	—	kHz
	Pass band edge frequency	—	4.5	—	kHz
	Stop band edge frequency	—	8	—	kHz
	Pass band ripple	—	5	—	dB
	Stop band attenuation	28	48	—	dB
DAC	Resolution	4	6	10	Bits
Generic	Supply voltage	—	1	—	V
	Process	—	60	—	Nm

Table 1:- CTDSP System Specification

The sampled outcome in aliasing more periodicity terms to the range of interest even if the Nyquist theorem is followed up and if a difference from the exact time instance can be due to the clock jitter and clk skew. This means a band-limiting filter known as an anti-aliasing filtering is necessary to escape an alimentation that could also costly implementation. Continuous times operates in digital signal processors [2,6] as a time in continuous or event based digital signal processor. The CTDSP system processes the input signal, X(t), which produces y(t). No clock in the system is involved. There are three basic sub-systems that can divide a CT system: CTADC, CTDSP and CTDAC.

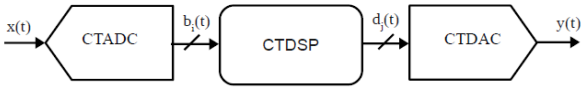

Fig 2:- CTDSP System with the Basic Model.

The digital signal processor in continuous time System uses a steady sampling approach, which generates samples only whenever occurrence crosses the predefined note level of quantization. A conventional DSP system uses a uniform technique to quantify and process samples at each clock cycle. The maximum input signal frequency determines the minimum sample generation clock frequency possible. However, exhausting samples are not necessary as in conventional systems in terms of signals are burst-like nature and long period of process. There is no information or repetitive information to the generated samples. Moreover, the terminating of such specimen by the signal processor in digital section requires additional dynamic power. The measurement steps it is possible to regular or uneven and can be further customized on the basis of their application. A CTDSP sub-system processes the digital continuous output, bicycle t, of the CT analog

converter block. adc output is digital so both processor and continuous time systems benefits are same. In [6] is described the conceptual approach to the CTDSP system. It can be built with multipliers, additives and delay taps as basic construction blocks based on the transmitters. A digital CT mode signal processor can be mapped from the discreet counterpart by substituting these blocks with the one of CT domain. For instance, the system can be used with non-synchronous factors and adders operating unless a clock. The delay taps are carried out using an inverter chain. In [9, 10], the data are collected with series-connected cells to delay and maintain data, thus providing a better approach. A handshake is used for correct transmission between delay cells. Experimentally confirmed by[4, 11] is the use of these delayed blocks.

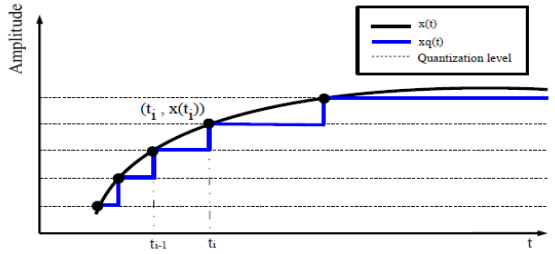

Fig 3:- CTDSP System for Level-Crossing Quantization Technique

III. EVENT DRIVEN ANALOG CONVETERS

The first module of the ED DSP system is the CTADC or ED ADC. The analog input signal, x(t), is converted by digital output signal from the Analog Interface (AI), $b_i(t)$. The AI section includes an analog filter and a sensor network. The sensor network detects and turns into electrical signals the variation of the input signal (temperature, pressure, moisture etc.). The analog filter limits the input signal frequency to the ADC operating range. The AI was developed according to the global smart dust modular specification for, for example, selecting the sensor interface based on application and selecting the analog filter's cut-off frequency based on an operating frequency of the system.

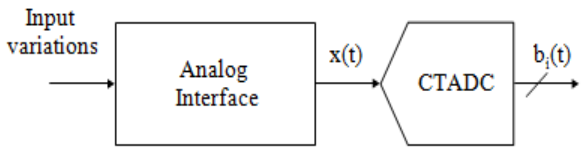

Fig 4:- Schematic Diagram of AI and ADC in Continuous Time Andai .

AI gives a x(t) signal to the CTADC block, as illustrated in Fig. 4. The CTADC consists of a quantizer in continuous time and a digital encoder for $b_i(t)$. The electronic output, $b_i(t)$, can be continuously displayed in various ways in accordance with the ADC architecture[3].The CTADC uses a sampling technique for level crossing. A detailed explanation of them crossing-level methodology is submitted. Illustration Displays the CTADC quantization process. When a quantization reference level is crossed by x(t), the input signal will be quantized at the closest quantization level based on the signal direction. As shown in Fig. 5 the quantized signal $x_q(t)$ is continuous over time and the samples are shown

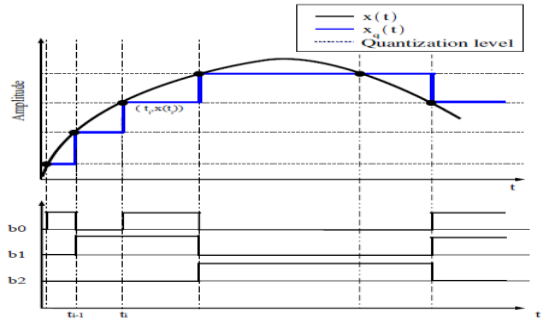

Fig 5:- Level-Crossing Quantization in the CTADC with 3-Bit Digital Output

An ED digital converter comparing two comparators: a DAC response System, the two-way SR and a digital control system asynchronous. Fig.6 shows the block of the ED DMADC system. Two reference signals are generated by the DAC: V_{up} (t) and $V_{down\ t}$(t) for both the top and bottom comparator; When the input signal is larger (less) than the V_{up} (t)(V_{down}(t)) and zero when the signal is between the two reference levels, the upper (less) comparator tracks the positive (negative) going signal and produces output Inc(Dec) which is high. Digital asynchronous control logic generates signals based on the Inc / Dec value: change and direction, which is collectively referred to as the "data token." it gives bi-directional SR, which increases (decrements), while signal is high, the DAC output, $V_{up}(t)$ and $V_{down}(t)$, by (VDC voltage resolution).

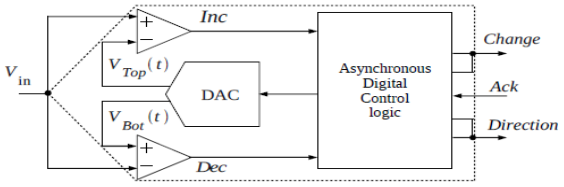

Fig 6:- Event-Driven ADC Based on Delta Modulation Technique

IV. CONTINUOUS TIME SIGNAL PROESSORS

Once the input signal received by the sensor is quantized by CT, it needs to be processed in order to deduce data content of the quantized and digital tokens. Before data transmission, processing is performed with a digital signal processor. This can be done in CT or discrete times. In order to avoid sampling clock and associated inconveniences, the CTDSP is preferred over the conventional sampled system. For the design of the CTDSP, the CTFIR filter is considered. Analysis and simulation of digital signal processorsin continous time[7] it processing of signals can be done in the digital domain with basic blocks like adders, multipliers and delay

elements, all of which run continuously. The use of a DMADC is an approach. The two signals that form the DMADC output data token collectively are turned to direction. The change is a time examples of sample generation and the direction shows the "more" or "less" signal value. Say that digitalization signal is totally N-bit and can be rebuilt getting back to the quantization signal q(t). Modified instructions are called as a data token ([change, direction]) collectively from now on. As illustrated in Fig.7, the data token is passed on to the counter that is [1,1] or [1, 0] in or down by 1 LSB. The counting up or down can only done if single LSB of the past value stored in the counter has been added or subtracted from. The output from the q(t−k. T_D) and expended by b_k, which produces output, $m_k(t)$, as specified by tap coefficient And the final output, y (t), it is weighted sum of m_k (t), are given by

$$m_k(t) = b_k \cdot q(t\text{-}k\cdot T_D) \ . \quad (1)$$

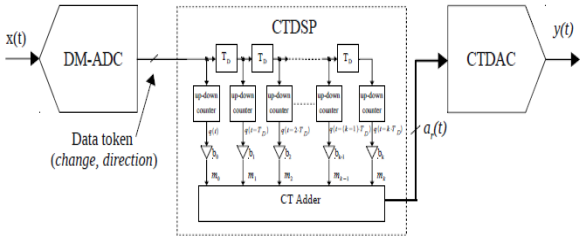

Fig 7:- Event-Driven FIR Filter with DM Encoding Technique

$$y(t) = \sum_{k=0}^{k} m_k(t) = \sum_{k=0}^{k} b_k \cdot q(t - k \cdot T_D). \quad (2)$$

A few basic design parameters required to design the CTDSP system are discussed in this section. A CTDSP system transfer function that filter deliver feature B(s), which we can determine by the output Laplace transforms, Y(t) as given through in which Y(t) is represented as the linear combination of an input signal quantified, q(t). Here Y(s) output of the system with frequency answer, B(s) and a quantation Q(s).

$$Z(s) = Y(s) \cdot B(s). \quad (3)$$

Z(s) can be written as

$$Y(s) = \left[\sum_{k=0}^{k} b_k \cdot e^{-s\cdot T_D\cdot k}\right] \cdot Q(s). \quad (4)$$

The CTADC data token depends on the pitch of the input signal. As it defines the functional demand of DSP section, a total number on data tokens generated is primary and minimum distance between the two tokens possible. In order to ensure the correct filtering operation by the DSP block, both number and distance between the two tokens must be preserved. If there is no data token or a distance deviation between the two tokens, the filter frequency response can vary unwontedly through the above case, f_b =21 kHz equals approximate 17MHz should be able to operate the CTADC rate of 1/Tone minute. This corresponds to a speed in 400 over-samples of ADCs. It is therefore changeable for less -frequency only, as the data token rate, which cannot be applied in a mainstream CMOS process, is very high for the large input frequency with that same oversampling ratio. Through power consumption of a CTDSP system can be defined roughly based on the aforementioned discussion and design parameters, f_b as well as N of the ADC.

V. DIGITAL COVETER IN CONTINOUS TIME

The CTDAC is the CTDSP system's final block. The CTDSP sub-system output is converted into an analog equivalent.DAC feedback is necessary within the CTADC block, as shown in Fig. 8. So the complete system here two DACs. A goal of design is to reuse both locations with a same framework. For this purpose, any DAC are works in asynchronous form. The following points to be taken into consideration when choosing a DAC architecture that is suitable for feedback as well as the output DAC are not enough: The CTDAC should produce two reference levels $V_{Top}(t)$ and $V_{Bot}(t)$. The two levels of reference are divided by the equation LSB (2)

$$V_{Top}(t) - V_{Bot}(t) = \Delta LSB \quad (5)$$

Note that for the DAC output only one output is required. To monitor input signal continuously in the DMADC, the output shall increase or decrease by only one bit at a time. They shall operate without a clock in asynchronous mode, since the other sub modules do not employ a clock

$$m = \begin{cases} n = 2^{N/2} \text{if N is even} \\ \frac{n}{2} = 2^{\frac{N-1}{2}}, \text{ if N is odd} \end{cases}. \quad (6)$$

$$\text{Here } \Delta_{MSB} = \frac{V_{ref,high} - V_{ref,low}}{m} \quad (7)$$

Where Δ is given b

$$\Delta = \frac{V_{ref,high} - V_{ref,low}}{m \cdot n} \quad (8)$$

The loading effect of the LSB string on the tapped MSB resistor however is explained in the next section, as described. Let R_{MSB} and R_{LSB} be the resistors of each MSB and LSB resistor string. The total LSB, R_{LSB}, Total resistance series is determined by that'sR_{MSB} different. Thus, the voltage drops across the MSB resistor as shown in Eq (6) is not exactly equal to that of the MSB. The result is that wrong reference voltages are generated at the DAC output. The LSB string loading effect can simply be avoided by adding buffering between the MSB and LSB string.

$$R_{LSB}, Total = n \cdot R_{LSB} \quad (9)$$

This means were indeed serial m resistors are most significant bit string and each resistor produces the same as that required as (6). Thus, the loading effect could be escape with the correct choice of LSB string resistors.

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VI. RESULTS

Fig. shows the output spectrum of the 3-bit system. As evident, the dominating frequency terms are the third and the fifth harmonics. The even order harmonicsaresuppressedbymorethan35dB.Also,there is no noise floor formed in this case as would have in conventional DSP system.

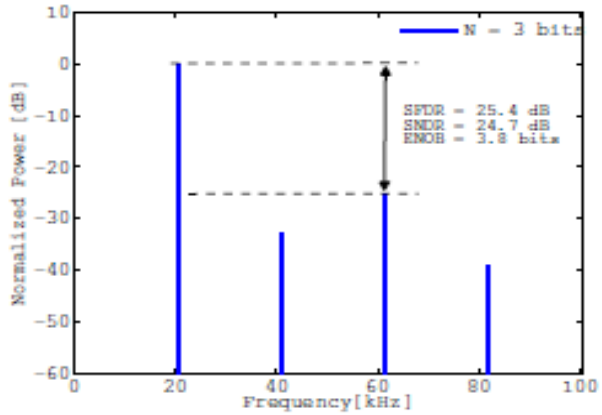

Fig 8:- Frequency Spectrum of 3-Bit CTADC System with Resistor- String DAC and 20.500 KHz Input Frequency Also 100 KHz Band of Interest.

Fig.8 shows a 3-bit system output spectrum. Results are observed similar to the 3-bit system. The dominant frequency component is a harmonic third order. As visible, the harmonics of even order are replaced by larger than 41 dB. Furthermore, the performance of the 4-bit ADC system is checked by introducing a 1-% disadvantage in the resistor string, where LSB resistance is 8kΩ. The SNDR is slightly different from its 34.1 dB nominal value. The incompatibility can be reduced by increasing the value of the resistance in both the MSB and the LSB strings, but this also leads to an increase in area and possibly thermal noise. Therefore, there is a need for proper trade between the two. The integration of the entire CT signal processor with different sub-systems is discussed in this chapter. The results are presented for 3-bit, 4-bit and 8-bit ADC systems. The SNDR for CTADC is higher than the standard Nyquist rate systems. The 8-bit CTADC resolution is not required for the smart dust application and the 3-bit resolution is sufficient to detect and process the signal present at the input of the smart dust. The lower resolution system also relaxes the DSP section, because it requires less hardware and thus reduces the total system power consumption. The complete 3-bit and 4-bit configuration CTDSP systems are designed, with CTADC, CTDSP and CTDAC presenting the basic subsystems and the results. It has been shown that the output of the entire CTDSP system is as intended and suitable for the application of intelligent dust.

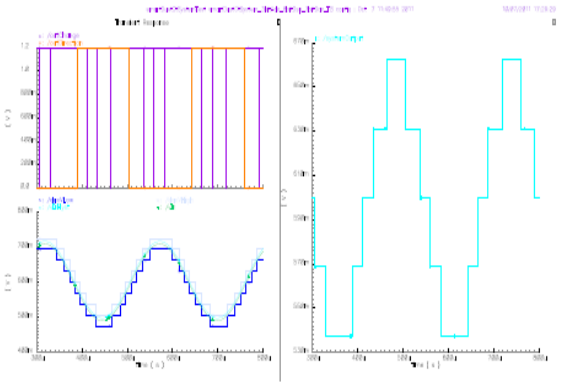

Fig 9:- Transient Response of the 3-Bit System.

The overall output of a system is shown on right side of the Fig.9 out Change and Direction are the tokens generated by a digital delta modulation or. The transient response of the CTDAC system is shown in Fig. for the input sinusoid of the frequency 4 kHz. The total system output is periodic. To check the frequency component in the signal's system Output signal frequency spectrum.

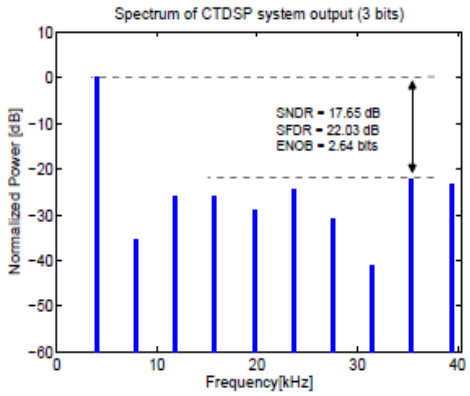

Fig 10:- Output Frequency Spectrum of 3-Bit CTDSP System

Fig.10 shows the system Output signal frequency spectrum for a 3-bit system. The frequency band is regarded as 40 kHz. It can be observed that the 4 kHz input signal is recovered from the system output.

VII. CONCLUSION

A detailed study of the CT DSP systems based on the level crossing or the ED sampling system will be presented in this research. It is illustrated that clock less CT quantizes exhibit very less quantification noise than conventional clocked DSP systems, only in the form of in-band harmonics. No aliasing effects are observed, because there is no sampling at all. It has been demonstrated that data acquired using CT can be processed using a digital signal processor in continuous time mode. The DSP section is made up of asynchronous blocks with extensive handshakes. That is concluded CT processing is very suitable for application of intelligent dust. The system's noise immunity is provided by adding an offset of Δ / 4 to the lesser CT analog converter. An ADC input using a level

crossing sampling system is described and a CT low pass FIR filter is used. The CTDSP system is simulated with a 4 kHz frequency sinusoid input and the SNDR obtained at the 3-bit CTDSP output is 17.65 dB respectively. The CTADC or ED analog converter and DSP in continuous time can be presented as potential field and energy saver are demonstrated as appropriate for smart dust applications and wireless applications.

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