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Comparative Study of Conductance Differential Solution using Threshold Logic

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Abstract:- Threshold logic is used for achieving high throughput, low power dissipation, and also provide effective improvement in reducing gate count, pipelining, and number of interconnects. Digital circuits are mostly implemented by means of Boolean logic. However, Threshold logic (TL) is an another way to implement Boolean logic functions. A single threshold gate is able to implement complex Boolean logic functions. This project proposes a Comparative study of power using threshold logic in conductance/current implementation.

Keywords:- *Threshold Logic, Boolean Functions, Low Power.*

I. INTRODUCTION

In VLSI technology, more than thousands of active and passive electronic components like transistor, diodes, FETs, resistors, capacitors, filters, etc., are integrated inside. The optimal minimization of power consumption, propagation delay and occupational area are the main requirement of VLSI based design. VLSI finds application in all aspects of life, like consumer electronics, defense, computer, communication electric circuits and networking etc.

Minimizing the area and dynamic power of digital CMOS circuits have always been two central objectives of the automated circuit design. This focus on dynamic power stems from several problems arising from increased power consumption. First and foremost are thermal constraints. The increased temperature of circuits has several debilitating effects such as reduced speed, increased leakage (wasted power), accelerated aging etc. Reducing power consumption not only alleviates these problems but also reduces packaging and cooling costs. The second requirement for low power comes from limited energy capacity of batteries used to power mobile devices. As more and more transistors are packed on today's chips, the power requirement starts growing beyond the capabilities of the batteries necessitating energy-efficient designs. Improvements in battery technology to increase their capacity have not kept pace with the increase in transistor count and transistor density made possible by technology scaling. Energy efficient design is therefore critical for mobile platforms. Efforts to reduce power consumption of digital CMOS circuits have been in progress for nearly three decades. As a result, a number of well understood and proven techniques for reducing dynamic and leakage power have been incorporated into modern design practices and tools.

Let the inputs of threshold gate are X_1, X_2, X_3… X_n. The corresponding weights of these inputs are W_1, W_2, W_3… W_n. The symbol of Threshold gate is shown in the following figure 1.

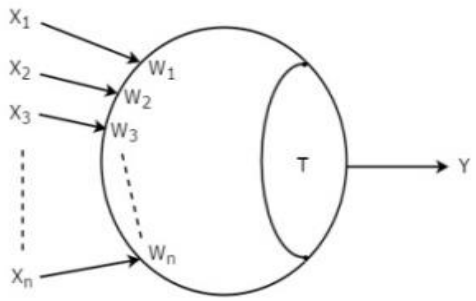

Fig 1:- Symbol of Threshold Gate

Threshold Gate is represented with a circle and it is having 'n' inputs, X_1 to X_n and single output, Y. This circle is made into two parts. One part represents the weights of the inputs and other part represents Threshold value, T.

The sum of products of inputs with corresponding weights is known as weighted sum. If this weighted sum is >= to Threshold value, T then the output, Y=1. Otherwise, the output, Y=0.

Mathematically, the relationship between inputs and output of Threshold gate as below.

$$y = \begin{cases} 1 & \text{if} \quad \mathbf{w}^T\mathbf{x} = \sum_{i=1}^{n} w_i x_i \geq T \\ 0 & \text{otherwise} \end{cases}$$

In this paper the comparative study of conductance Differential threshold logic is described. It consists of three types (section II) along with the characterization of the set of functions realized by threshold logic. The analysis of power and delay characteristics using threshold logic (section III), and the conclusion are present in section IV.

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II. PROPOSED CONCEPT

❖ *Conductance Differential Solution*

Many conductive threshold logic implementations, while fast and easy to implement using standard CMOS processes, are plagued by the issue of static power dissipation. While clocking mechanisms have been employed to eliminate static power during one phase of the clock or for certain combinations of inputs, one cannot expect widespread application of threshold logic until all sources of static power dissipation are eliminated from the gate. A subfamily of conductive logic gates that are able to achieve this goal are differential threshold logic gates.

A. Single Input Current-Sensing Differential Logic (SCSDL)

Single Input Current Sensing Differential Logic (SCSDL) is structurally very similar to LCTL, essentially a reordering of the devices in the pull down of the two differential branches of the logic element. The schematic circuit of SCSDL is shown in figure.

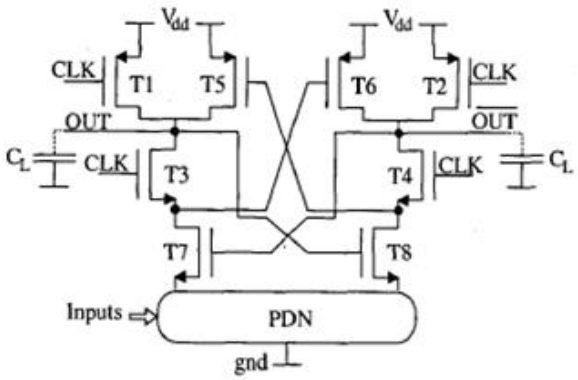

Fig 2:- Schematic of the SCSDL Gate.

Transistors M1-M8 comprises the differential amplifier portion of the gate, while transistor banks M9, M10 provide the networks of parallel input transistors. When the signal clock assumes logic 0, the gate is the reset phase of operation. Transistors M5 and M6 are inactive, thus neither of the internal nodes N1, N2 of the gate possess a conducting path to ground. Transistors M1 and M4 are active, thus nodes N1, N2 are pre-charged to logic 1. Any signal assignment provided to the SCSDL element assumes that there is at least one active device in both M9 and M10 at all times, thus nodes N3-N6 are discharged to ground during reset. When the signal clock rises to logic 1, the gate begins the evaluation phase of operation, In the evaluation phase, transistors M1 and M4 become inactive, while transistors M5 and M6 become active, causing nodes N1 and N2 to begin discharging to ground through devices M5-M10.

B. Differential Current-Switch Threshold Logic (DCVS)

Differential Current Switch Threshold Logic incorporates the improvements provided by SCSDL while adding additional devices to reduce the propagation delay of the logic element. The device level schematic of the DCSTL gate is shown in Figure 3.

Transistors M1-8 comprises the differential amplifier portion of the gate, while transistor banks M9-10 provide the networks of parallel input transistors. As with previous implementations of differential threshold logic.

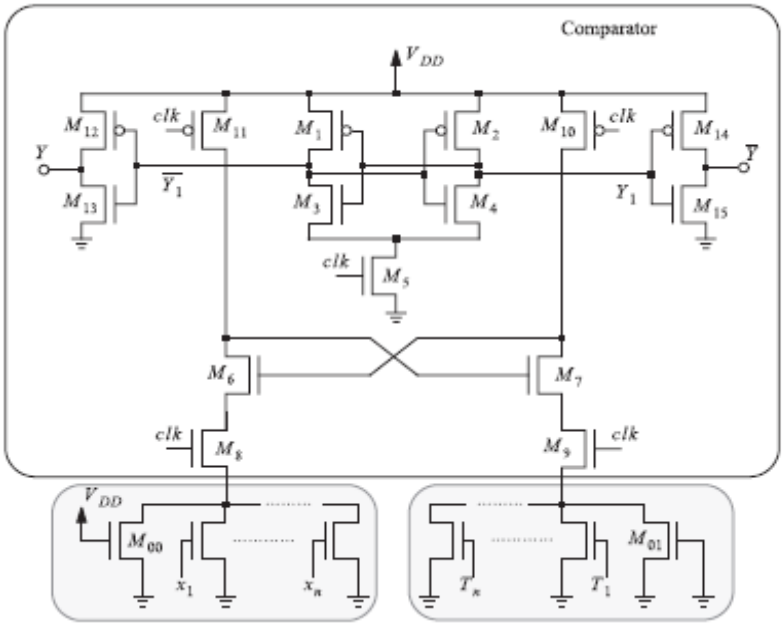

Fig 3:- Schematic of the DCSTL Gate

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- **Precharge:** when the signal clock assumes logic 0, the gate is in the reset phase of operation. Transistors M7 and M8 are inactive, thus none of the internal nodes N1-4 of the gate possess a conducting path to ground. Transistors M1 and M4 are active, thus nodes N1-4 are pre-charged to logic 1. Assuming there is at least one active device in both M9 and M10, nodes N5 and N6 are discharged to ground during reset.

- **Evaluation:** When the signal clock rises to logic 1, the gate begins the evaluation phase of operation. DCSTL uses the same placement of the input networks proposed by SCSDL, at the bottom of the discharge path (rather than the middle as in LCTL or the top as in CIAL). Additionally, the gate introduces transistors M11-13, which provide parallel discharge paths to nodes N1 and N2. These parallel discharge paths, while not required for proper operation of the gate, improve the performance of the gate by reducing the total discharge impedance observed by nodes N1 and N2.

C. Current-Mode Threshold Logic (CMTL)

The main advantage of using this circuit is its high performance and low power consumption. For resulting high performance selecting transistor configuration which can sense a small difference in current and also set the differential outputs to the correct values. Reduced power dissipation is achieved by limiting the voltage swing on the interconnects and the internal nodes of the CMTL gates. PMOS based CMTL gate received low swing inputs, which are sensed by CMTL gate and performs the logic computations. The full-swing outputs are used as inputs to the NMOS based interconnect driver. This basic circuit face a problem of static short-circuit power dissipation in the equalize phase and at the end of evaluate phase. This can be overcome by adding two additional PMOS transistors on the path from Vdd to the output nodes. This will result in the generation of two different transistor configurations discharge current mode threshold logic and equalized current mode threshold logic.

The block diagram of the CMTLG is shown in Figure 4. It consists of two parts. They are sensor part and differential part. The differential part is again divide into two parts, they are i) Threshold Part ii) Input part (+ve).

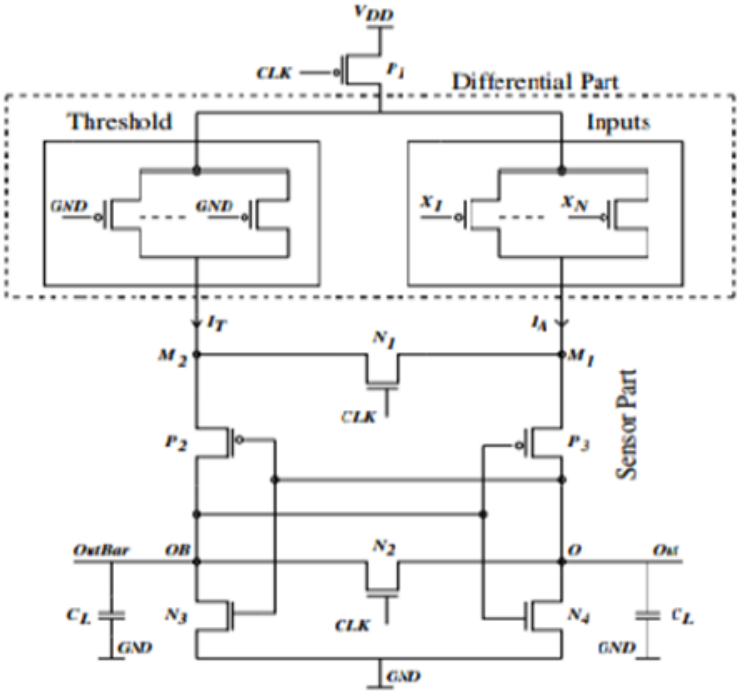

Fig 4:- Block Diagram of CMTL

The operation of the CMTLG take place into two phases, they are i) equalization phase ii) evaluation phase.

When the applied clock=1, then the circuit is in the equalization phase. When clock =0, then the circuit is in the evaluation phase. In the equalization phase, the transistors N1, N2 = ON, nodes M1, M2 is in similar voltage respective of transistor N1, and nodes O, OB also have the same voltage respective of transistor N2. In the evaluation phase, the transistors N1, N2 = OFF, the voltage at node O increases faster than node OB. If during the evaluation phase the threshold current exceeds the active current, then the voltage at node OB increases faster than node O.

An alternative differential clock threshold logic implementation is named as the Differential Current Mode Logic (DCML). The block diagram is shown in Fig.5

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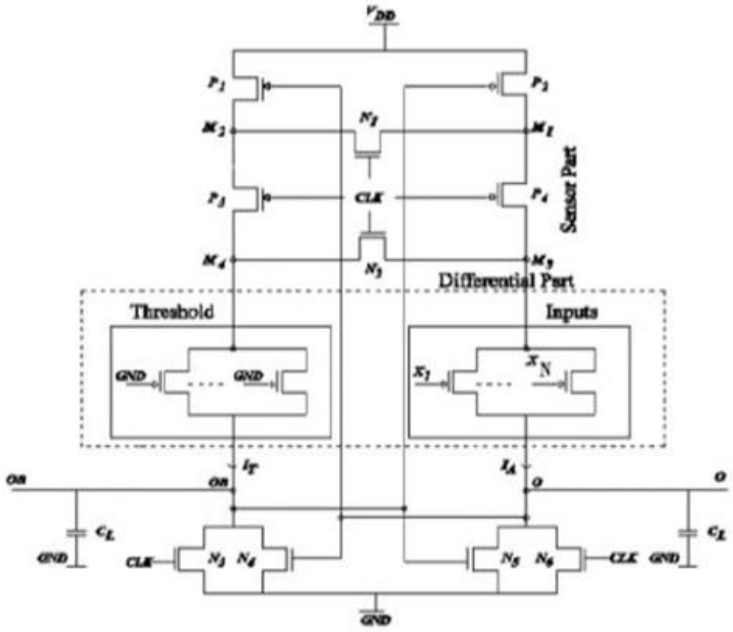

Fig 5:- Block Diagram of DCMTL

DCMTL is also subdivided into two parts; they are i) differential part ii) sensor part. The current through the threshold part is denoted by IT and the inputs part is denoted by IA. The sensor part contains four PMOS transistors, named as P1–P4, and six NMOS transistors, named as N1–N6. The load capacitance CL is applied to the output node O and node OB.

When the applied clock=1, then the circuit is in the equalization phase. When clock =0, then the circuit is in the evaluation.

III. RESULT AND DISCUSSION

In this section, the following comparison table (Table 1) shows the performance of different design using TANNER EDA tool.

PARAMETER		POWER (pW)	DELAY (ns)	PDP
SCSDL		2.69	2.51	6.7519
DCVS		1.8842	2.62	4.936
CMTL	CM	1.7976	2.43	4.368
	DM	1.7976	2.16	3.8828

Table 1:- Performance Analysis

From the table 1, SCSDL achieve 2.69pW power and 2.51ns delay, DCSTL has 1.8842pW power and 2.62ns delay, common mode CMTL achieve 1.7976pW power and 2.43ns delay, differential mode CMTL achieve 1.7976pW power and 2.16ns delay. It is clear from that, the current mode threshold logic (Differential Mode) provides better performance in terms of power and delay as compared to all the other logic. Therefore, CMTL is suitable for designing low power, high speed digital.

IV. CONCLUSION

In this paper, the performance Comparison of Conductance Differential Solution using Threshold Logic was performed. Apart from that Current Mode Threshold Logic (CMTL) achieve much power consumption when compared to other. The proposed method results in ultra-low power consumption. The workability of these circuits had been performed by Tanner Tool in 90nm and 70 nm CMOS Technologies.

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