ISSN No:-2456-2165

Analysis of New Topology for 7- Level Asymmetrical Multilevel Inverter and its Extension to 19 Levels

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Abstract:- Inverter is a power electronic device used to convert dc power into ac power at desired frequency and desired voltage level. Being a power electronic device, and due to absence of any rotating part and high switching ability, it is more efficient and reliable. Now a days an inverter is not only a device but also has become an important part of power industry but a simple inverter has only two level so the out coming wave is much distorted form fundamental sine wave of same time period and frequency which introduces the harmonics into the circuit which makes the total system less efficient along with that the heating effect of harmonics affects the age of system, also there is a danger of faulty operation [1,8]. As the presence of harmonics in the system have heating effect along with distortion which is not good for load as well as whole power system. So the concept of multilevel inverter came into existence in which the levels of the inverter is increased so that the distortion of the out-coming wave could be minimized [2].as the level rises the sinusoidal nature of the output wave increases and thus harmonic content decreases. In this paper a new asymmetrical multilevel inverter topology for 7 Level Inverter is proposed and its operation is being discussed and topology extended to 19 Level Inverter.

Keywords:- *Multi Level Inverter (MLI), Pulse Width Modulation (PWM), Phase Deposition Pulse Width Modulation (PDPWM),Phase Opposition Deposition Pulse Width Modulation (PODPWM), Alternate Phase Opposition Deposition Pulse Width Modulation (APODPWM).*

I. INTRODUCTION

An expansion of inverters to more than two levels to reduce distortion from fundamental sinusoidal waveform leads to concept of multilevel inverter. In present era of power sector MLI (Multilevel inverter) found its too much application especially in medium power applications. As they are capable of handling high voltages and power with reduced harmonic distortion [2, 3, 8]. Multilevel inverters are the devices in which the voltage across the load is measured and DC voltage sources being deciding the levels. And the circuit in one complete wave cycle for different duration is completed through different paths by using different switching arrangements. In this paper a topology for 7- Level inverter is examined and its results are compared with conventional symmetrical H-bridge type multilevel inverter extended to 19 levels. Moreover we have discussed inverted sine wave pulse width modulation technique and compared it with different existing modulation techniques viz. PD, POD, APOD etc.

II. CONVENTION TOPOLOGIES FOR SYMMETRICAL MULTILEVEL INVERTERS

Basically, multilevel inverters are of two types first is symmetrical multilevel inverter and asymmetrical multilevel inverter In case of later there can be number of arrangements and in case of former there are three arrangements first is diode clamped multilevel inverter second is flying capacitor type multilevel inverter and third is H-bridge type multilevel inverter [4,5,6,8] . Although they can also be classified according to number of phases which is also done in two i.e. three phase multilevel inverter and single phase multilevel inverter in this paper we are only concerned with single phase multilevel inverter. Basically there are three topologies which are as follows:-

- **Diode clamped multilevel inverter**
- **Flying capacitor multilevel inverter**
- **H-bridge type multilevel inverter[6,7]**

➢ *Proposed Topology: Proposed Topology for 7 Level Inverter*

A new a symmetrical topology is being proposed in this paper in which a dc voltage sources are used in which one is used in reverse direction and another is used in forward direction. The one which is used in reverse direction is of twice the magnitude of first. In our new proposed topology for 7- level inverter only 8 switches are used unlike figure 1 the switching arrangement for proposed 7- level inverter is shown in figure. Switching arrangement is shown in Table 1.

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OUTPUT VOLTAGE	S1	S2	S3	S4	S5	S6	S7	S8
+3	OFF	OFF	ON	ON	OFF	ON	ON	OFF
+2	OFF	ON	OFF	ON	OFF	ON	ON	OFF
+1	OFF	OFF	ON	ON	ON	OFF	ON	OFF
+0	OFF	ON	OFF	ON	ON	OFF	ON	OFF
-1	OFF	OFF	ON	ON	ON	OFF	OFF	ON
-2	OFF	ON	OFF	ON	ON	OFF	OFF	ON
-3	ON	ON	OFF	OFF	ON	OFF	OFF	ON

Table 1

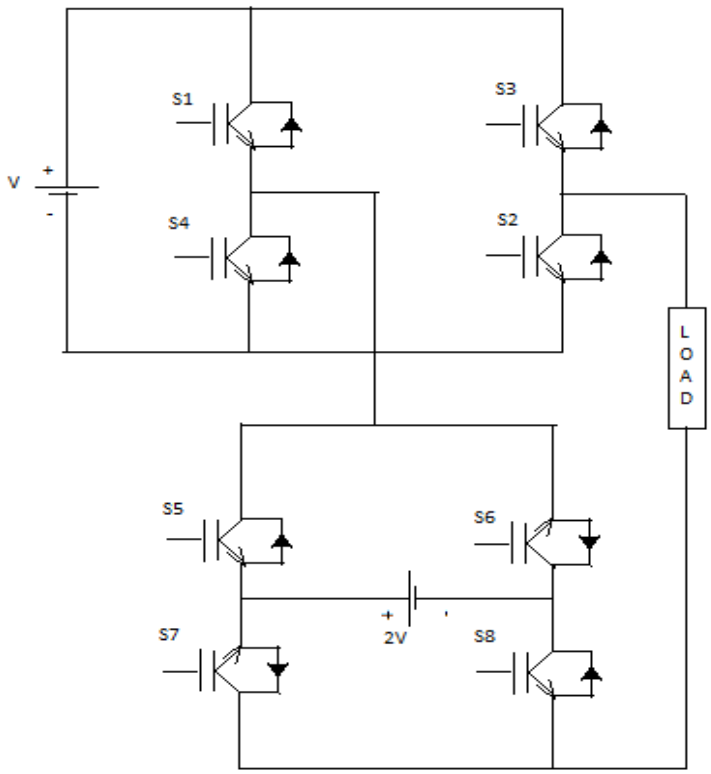

Fig 1

➢ *Modes of Operation for 7 Level Asymmetrical Multilevel Inverter*

In case of multilevel inverter the path is completed through load by opting different switching arrangements in order to attain different levels of 7 level single phase inverter. The current path for different levels are shown below in figure 2 (a, b, c, d, e, f, g) which is attained by switching as in table 1

Figure 2 (a) shows the current flow to attain +3V level , Figure 2 (b) shows the current flow to attain +2V level similarly, Figure 2 (c) , Figure 2 (d), Figure 2(e), Figure 2 (f) , Figure 2 (g) shows the voltage of +1V, 0V, -1V, -2V, -3V respectively.

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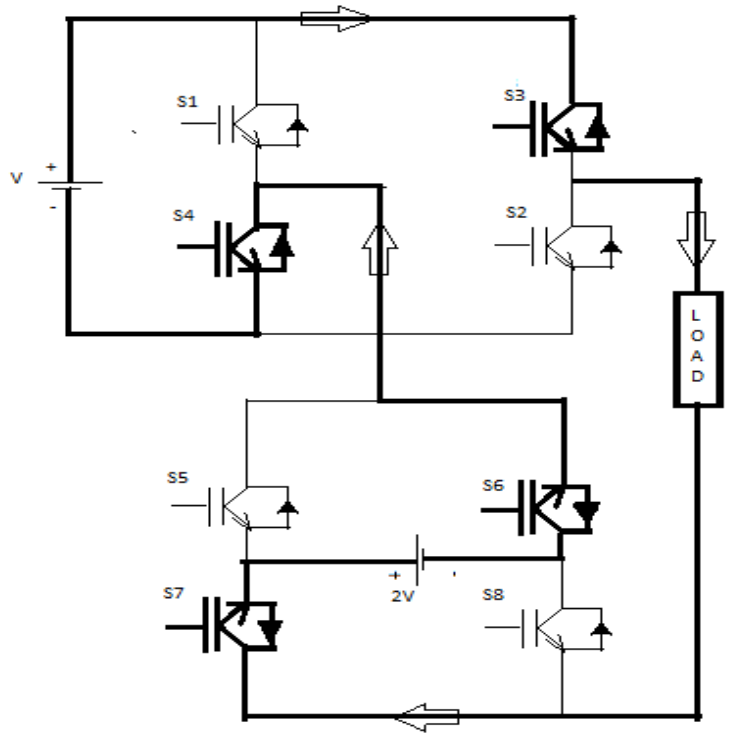

Fig 2(a):- +3V Level for 7 Level Inverter

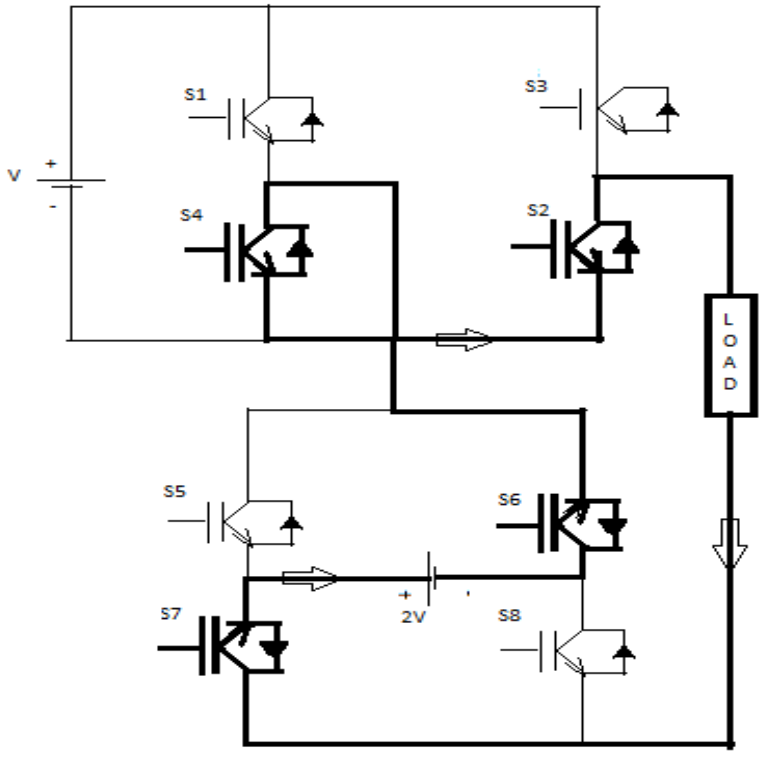

Fig 2(b):- +2V Level for 7 Level Inverter

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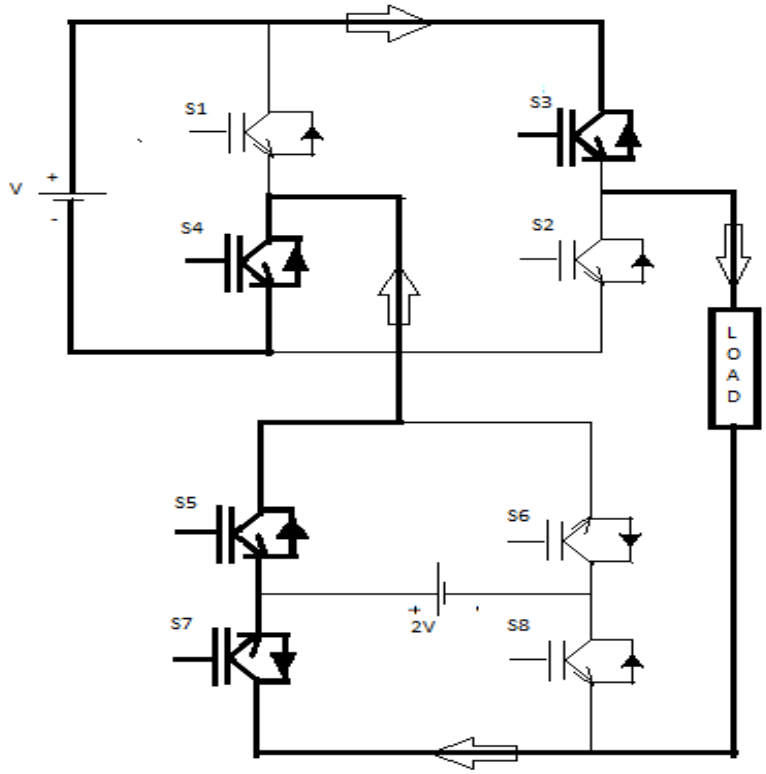

Fig 2(c):- +1V Level for 7 Level Inverter

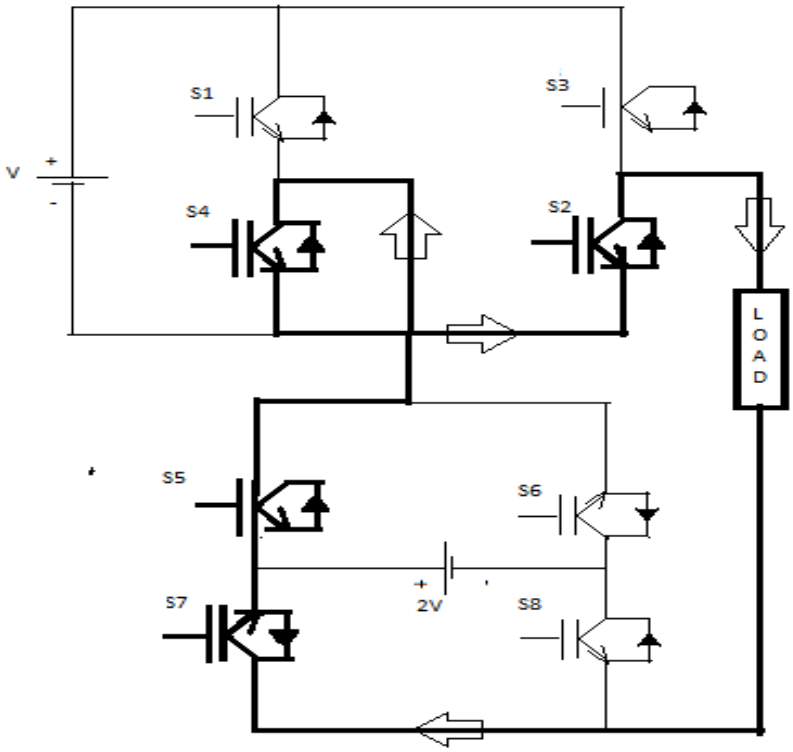

Fig 2(d):- +0V Level for 7 Level Inverter

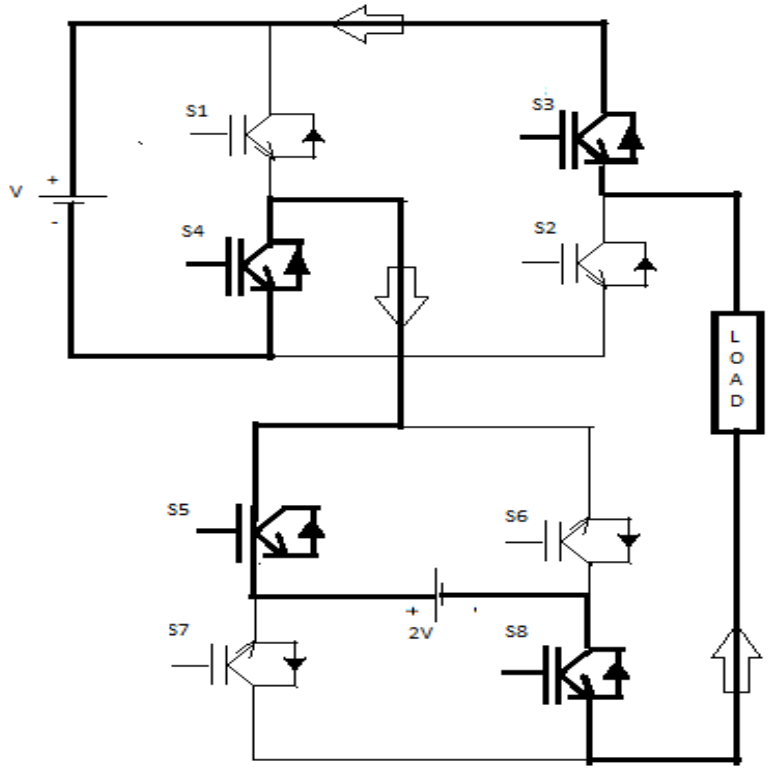

Fig 2(e):- -1V Level for 7 Level Inverter

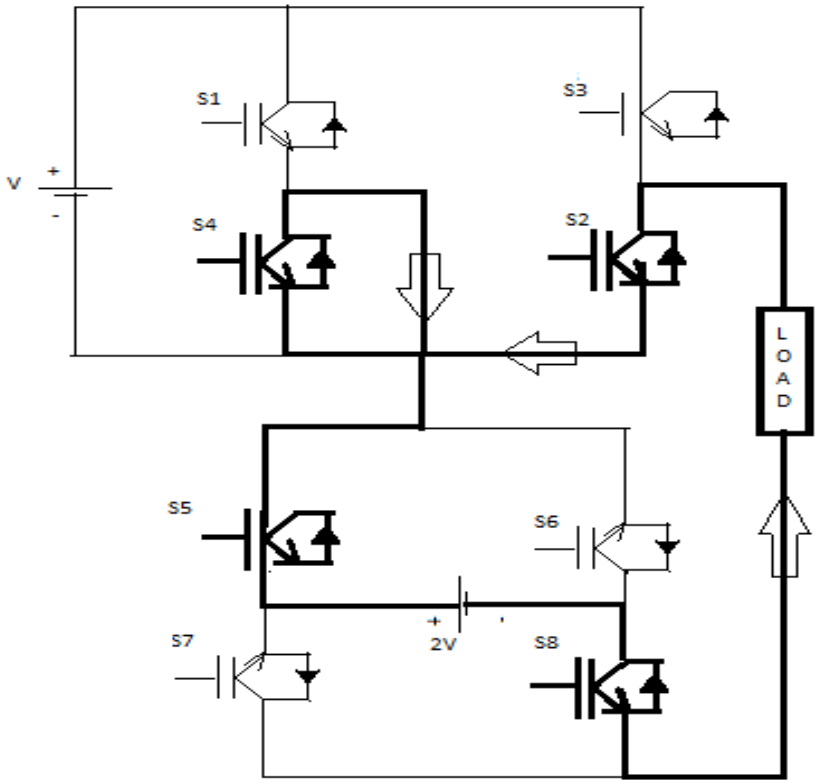

Fig 2(f):- -2V Level for 7 Level Inverter

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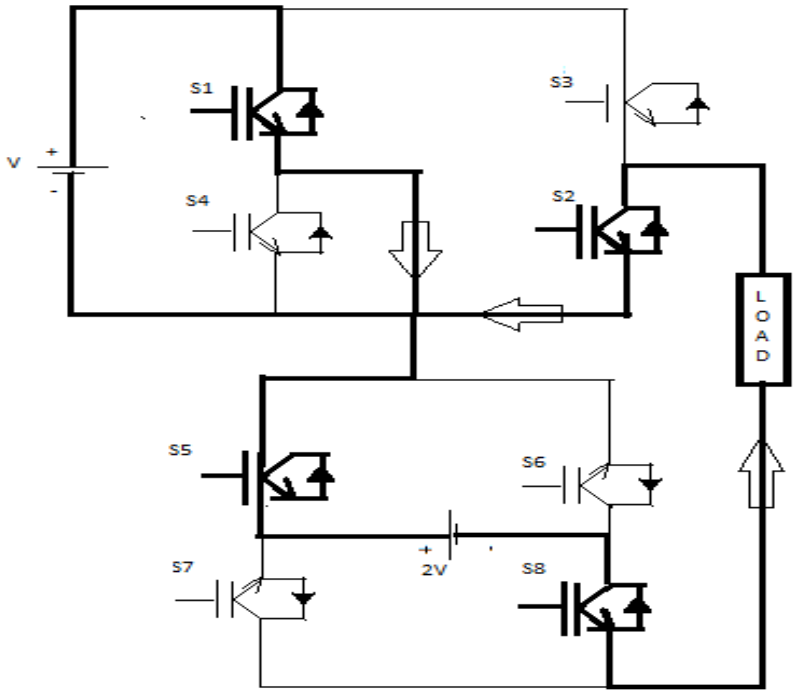

Fig 2(g):- -3V Level for 7 Level Inverter
Fig 2

➢ *Extension of Topology to 19- Level Inverter:-*

In case of 19 level inverter we use 12 switches and 4 voltage sources among which 2 are used in reverse direction as shown in figure 3 the voltage for the inverter need to be in levels +9L, +8L, +7L, +6L, +5L, +4L, +3L, +2L, +1L, 0L, -1L, -2L, -3L, -4L, -5L, -6L, -7L, -8L, -9L and the switching arrangements for different levels of multilevel inverters are shown in table 3 and obviously with the increase in level of inverter the harmonic content in our output wave decreases[6] so distortion is reduced as compared to lesser level inverters. The circuit diagram for 19 level inverter is shown in figure 3 in order to reach up to +9 level WITHIN VOLTAGE RAGE +3V TO -3V we uses the DC voltage source of 1V, 1V, 1/3V2/,3V

OUTPUT VOLTAGE LEVEL	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
+9	OFF	OFF	ON	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON
+8	OFF	ON	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON
+7	OFF	OFF	ON	ON	OFF	ON	OFF	ON	ON	OFF	OFF	ON
+6	OFF	ON	OFF	ON	OFF	ON	OFF	ON	ON	OFF	OFF	ON
+5	OFF	ON	OFF	ON	ON	OFF	OFF	ON	ON	OFF	ON	OFF
+4	OFF	OFF	ON	ON	OFF	ON	OFF	ON	ON	OFF	ON	OFF
+3	OFF	ON	OFF	ON	OFF	ON	OFF	ON	ON	OFF	ON	OFF
+2	OFF	ON	OFF	ON	ON	OFF	OFF	ON	OFF	ON	OFF	ON
+1	OFF	OFF	ON	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON

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+0	**OFF**	**ON**	**OFF**	**ON**	**OFF**	**ON**	**OFF**	**ON**	**OFF**	**ON**	**OFF**	**ON**
-1	**ON**	**ON**	**OFF**	**OFF**	**OFF**	**ON**	**OFF**	**ON**	**OFF**	**ON**	**OFF**	**ON**
-2	**ON**	**OFF**	**ON**	**OFF**	**OFF**	**ON**	**ON**	**OFF**	**ON**	**OFF**	**ON**	**OFF**
-3	**ON**	**OFF**	**ON**	**OFF**	**OFF**	**ON**	**OFF**	**ON**	**OFF**	**ON**	**ON**	**OFF**
-4	**ON**	**ON**	**OFF**	**OFF**	**OFF**	**ON**	**OFF**	**ON**	**OFF**	**ON**	**ON**	**OFF**
-5	**ON**	**OFF**	**ON**	**OFF**	**OFF**	**ON**	**ON**	**OFF**	**OFF**	**ON**	**OFF**	**ON**
-6	**ON**	**OFF**	**ON**	**OFF**	**ON**	**OFF**	**ON**	**OFF**	**OFF**	**ON**	**ON**	**OFF**
-7	**ON**	**ON**	**OFF**	**OFF**	**ON**	**OFF**	**ON**	**OFF**	**OFF**	**ON**	**ON**	**OFF**
-8	**ON**	**OFF**	**ON**	**OFF**	**OFF**	**ON**	**ON**	**OFF**	**OFF**	**ON**	**ON**	**OFF**
-9	**ON**	**ON**	**OFF**	**OFF**	**OFF**	**ON**	**ON**	**OFF**	**OFF**	**ON**	**ON**	**OFF**

Table 3

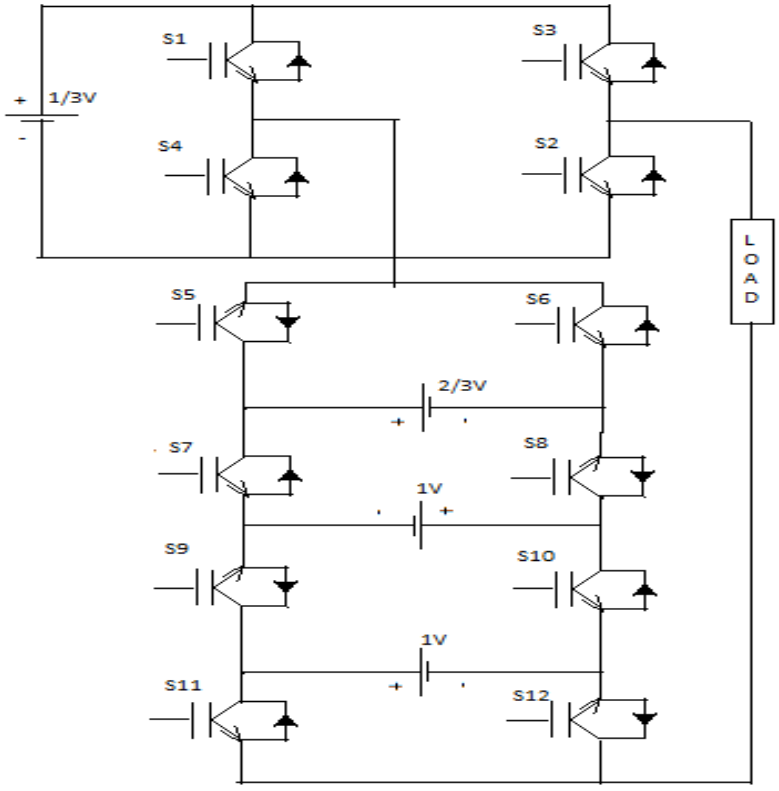


Fig 3

➢ *Simulation :*

In this paper power library of MATLAB is utilized to create models of MLI and then applied with discrete domain PWM. We have introduced a new topology in which we have taken a source of double magnitude in reverse direction in second bridge and source of first bridge in same direction [15] as shown in figure 12.

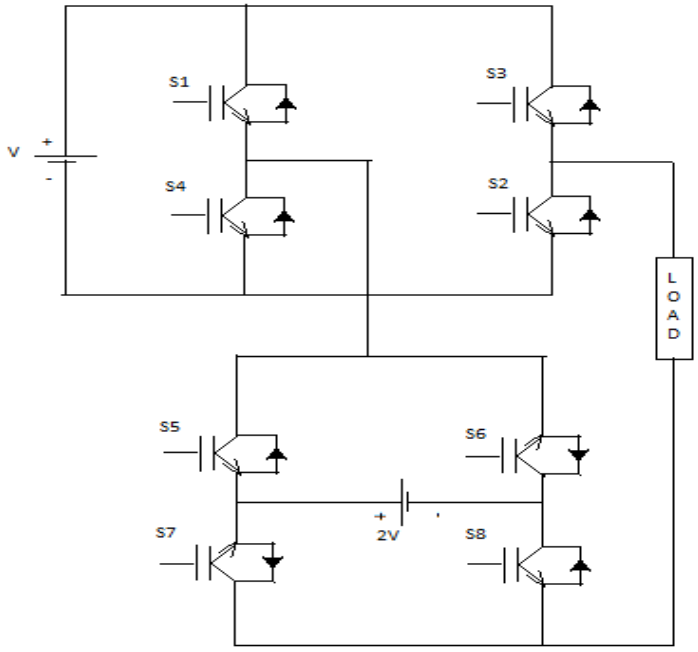


Fig 4:- Topology

In this chapter we are trying to study and also apply some innovative variable frequency method not to reduce total harmonics distortion, but also with aim to tackle the shortcomings faced by existing methodologies e.g. switching losses, differential switching losses etc.

- **PDPWM:-**

In Phase disposition pulse width modulation technique all carrier above and below the zero reference are in same phase[2,3,6,7].

➢ *Various PWM Techniques are:-*

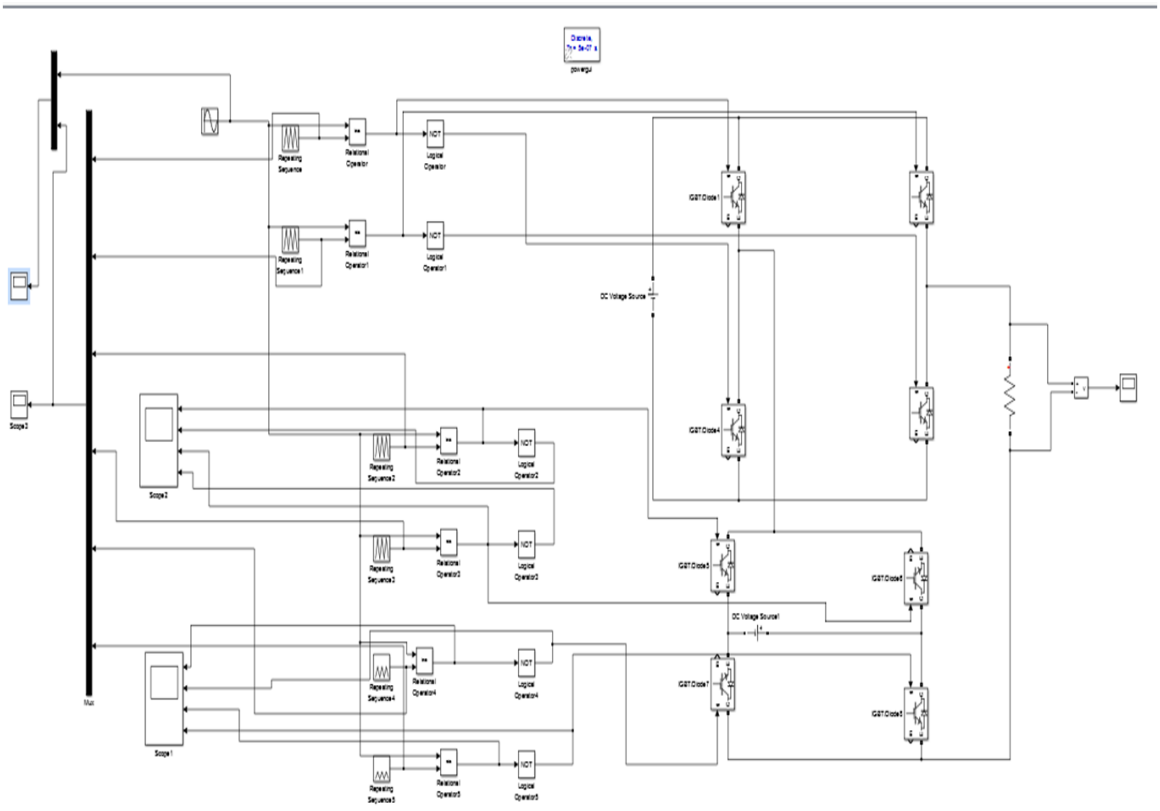
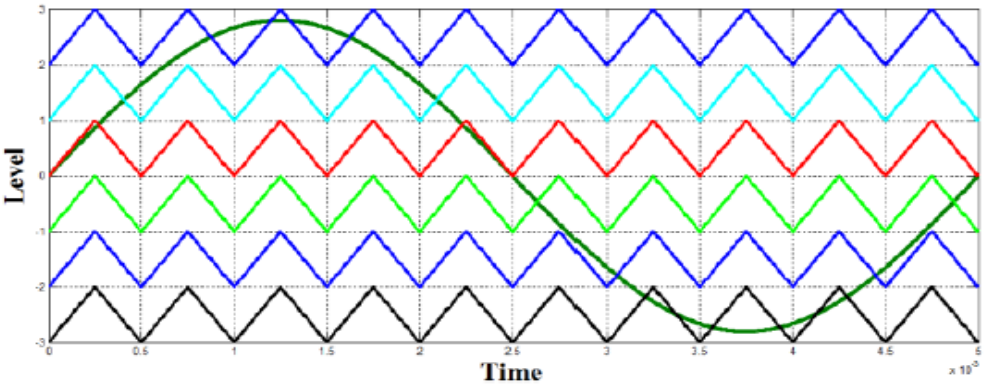
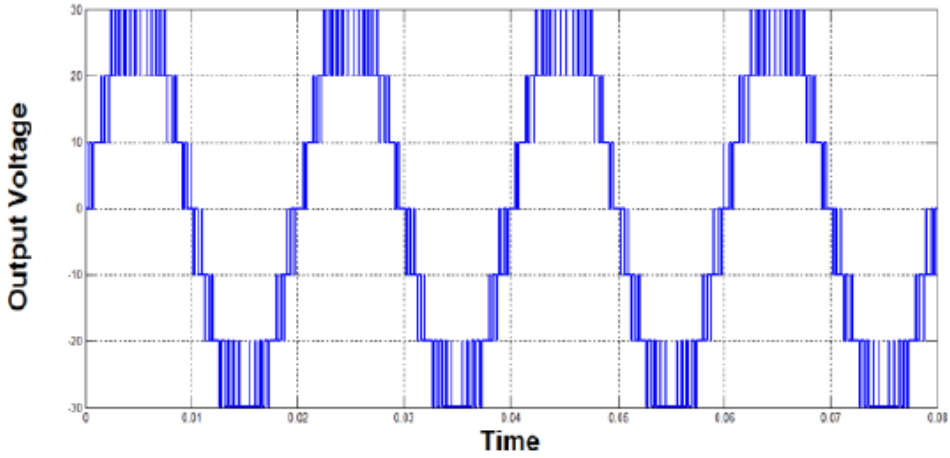


Fig 5:- 7 Level MLI used for PDPWM, POPWM, APODPWM & VFISPWM

- **PDPWM**



(a)

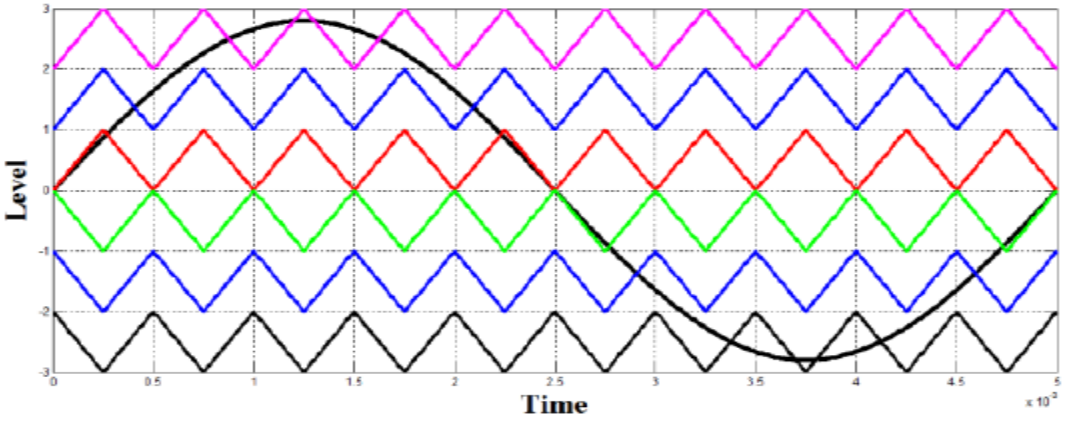


(b)

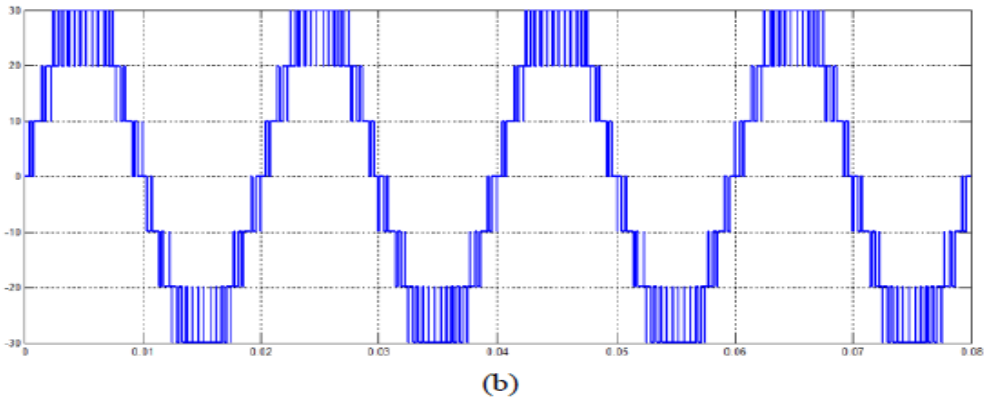
Fig 6:- (a) PDPWM Modulation Technique for 7 Level Inverter. (b) Output Voltage

The waveform shown in figure 6(a) is with lesser number of cycles instead of actually used ones just to make the changes visible otherwise graphics will become hazy.

- **PODPWM**:- In this modulation techniques all carrier above zero reference and below the zero reference also in same phase but 180° out of phase with above and below the zero reference[4,5,9].



(a)

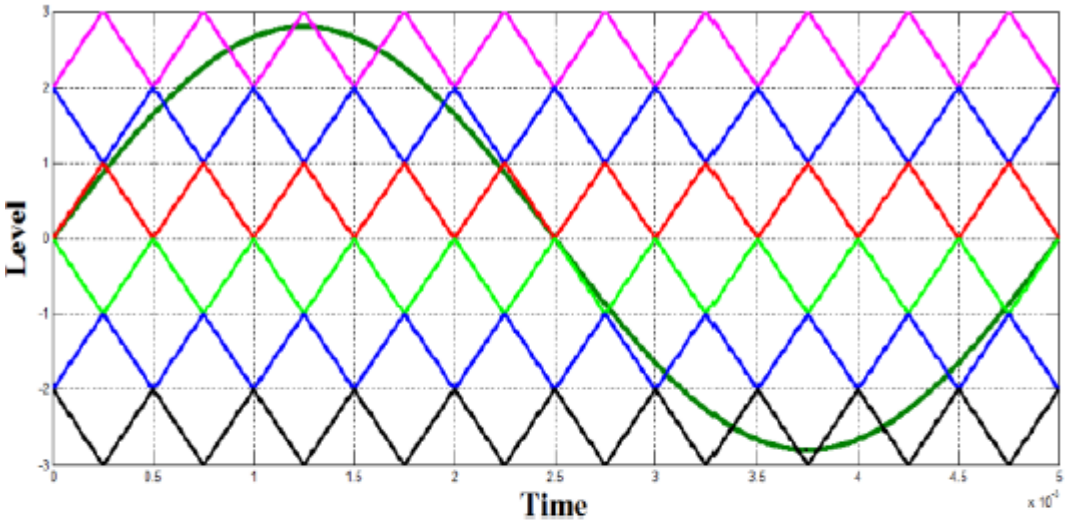


(b)

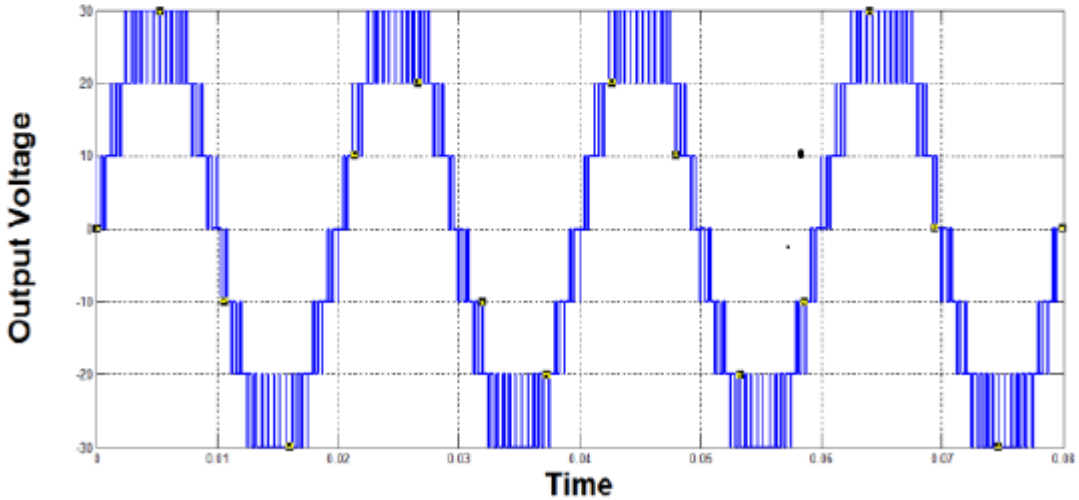
Fig 7:- (a) PODPWM Modulation Technique for 7 Level Inverter. (b) Output Voltage

The waveform shown in figure 7(a) is with lesser number of cycles instead of actually used ones just to make the changes visible otherwise graphics will become hazy

- **APODPWM:-** In alternate phase opposition Disposition pulse width modulation scheme every carrier is out of phase with its neighbor carrier by 180°[1,8,10].



(a)



(b)

Fig 8:- (a) APODPWM Modulation Technique for 7 Level Inverter. (b) Output Voltage

ISSN No:-2456-2165

The waveform shown in figure 8(a) is with lesser number of cycles instead of actually used ones just to make the changes visible otherwise graphics will become hazy.

➢ *Variable Frequency Inverted Sine Carrier PWM Technique (VFISC-PWM)*

In this new introduced technique we are applying the PODPWM technique but frequencies of the carrier wave signal is being modified or varied in such a way that the total harmonic distortion could be reduced.

The carrier signal is inverted sine with different frequencies at each band. The rationale behind varying the frequency is that we want to take more number of samples near the reference line and a gradual change in frequency in such a manner that the number of samples taken become lesser; and finally at near peak area only one sample is taken which covers the full outer periphery of part of the wave.

- ***For Seven Level MLI***

As we worked on 7 level inverter, through which we have to operate 50Hz system then for each level we will be using different frequency as mentioned in figure as well as table below.

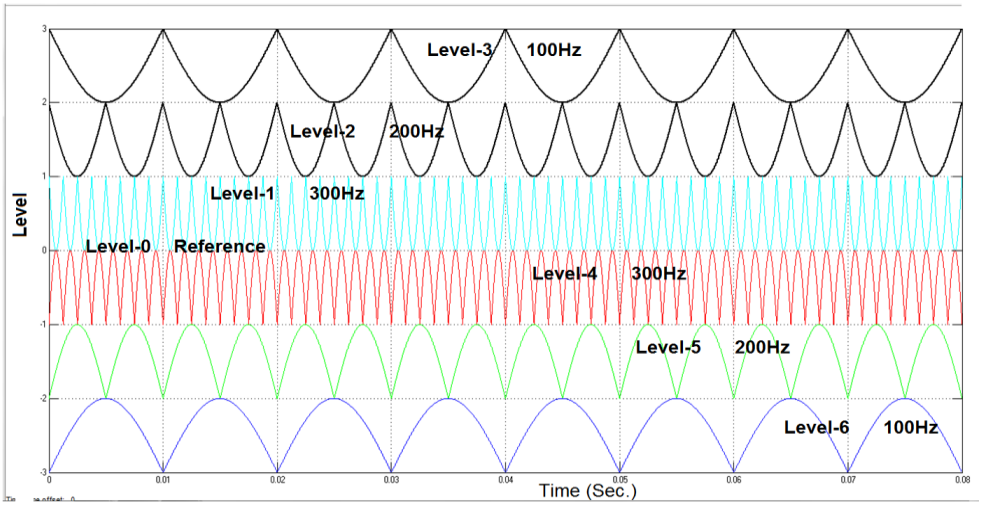


Fig 9:- Variable Frequency PWM Technique for 7 Level Inverter

➢ *Carrier Frequency for Different Levels for 7 Level Inverter*

Level	Frequency (Hz)
0	-
1	300
2	200
3	100
4	300
5	200
6	100

Table 4:- Different carrier frequencies for 7 level MLI

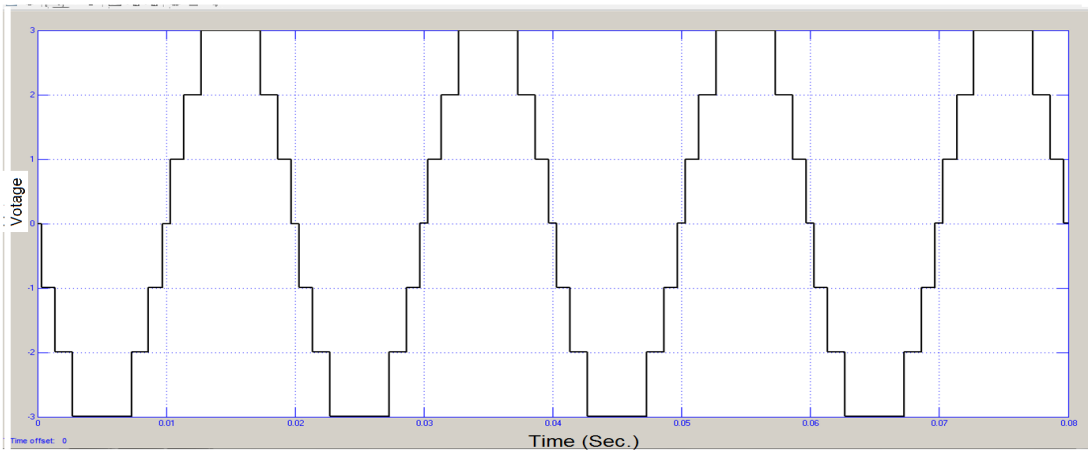


Fig 10:- Output Wave for 7 Level Multi Level Inverter

ISSN No:-2456-2165

Afterwards the FFT (fast Fourier transform) is obtained using matlab simulink and hence THD is compared with other methodologies. The THD is seen upto 1000Hz frequencies with respect to 4 cycles. The THD report is obtained in bar chart formate.

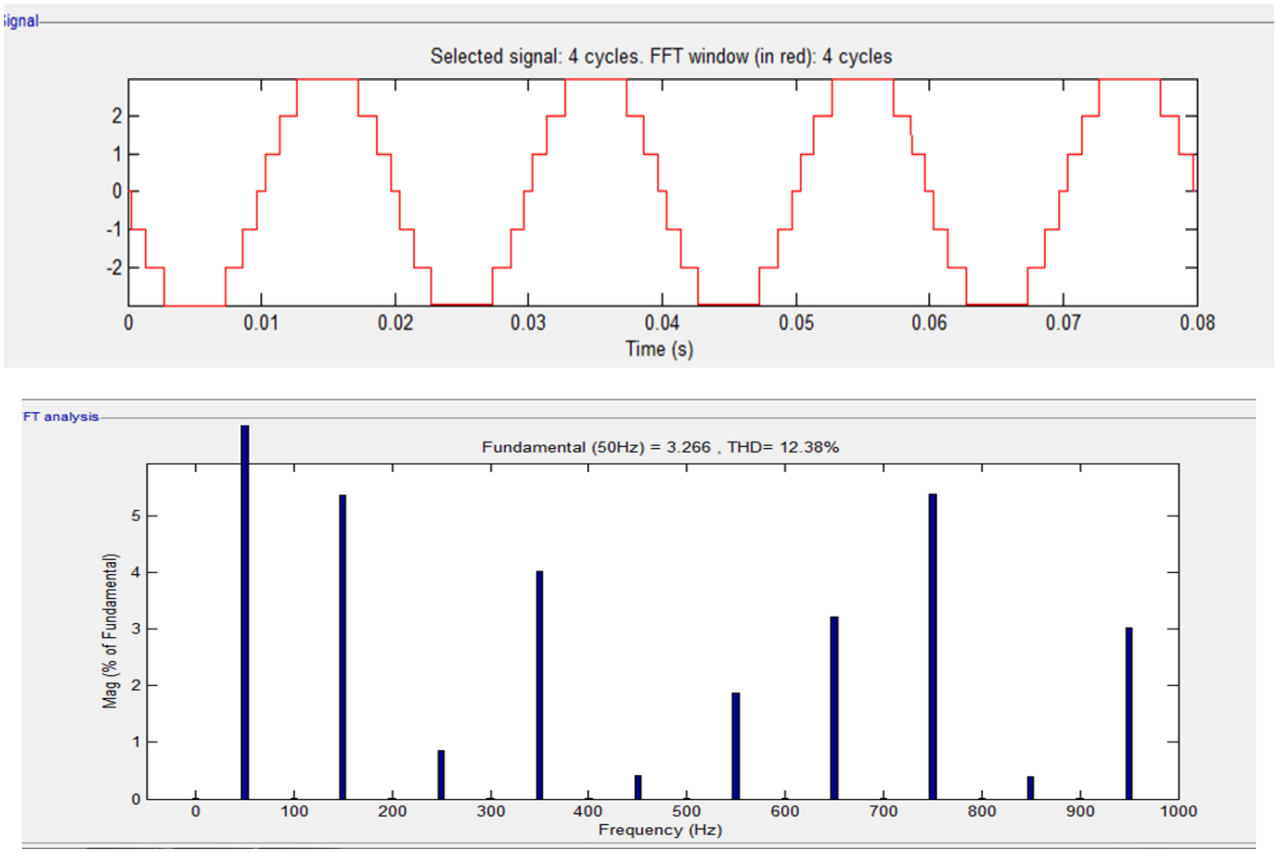


Fig 11:- FFT 7 level MLI

➢ *For Nineteen Level MLI*

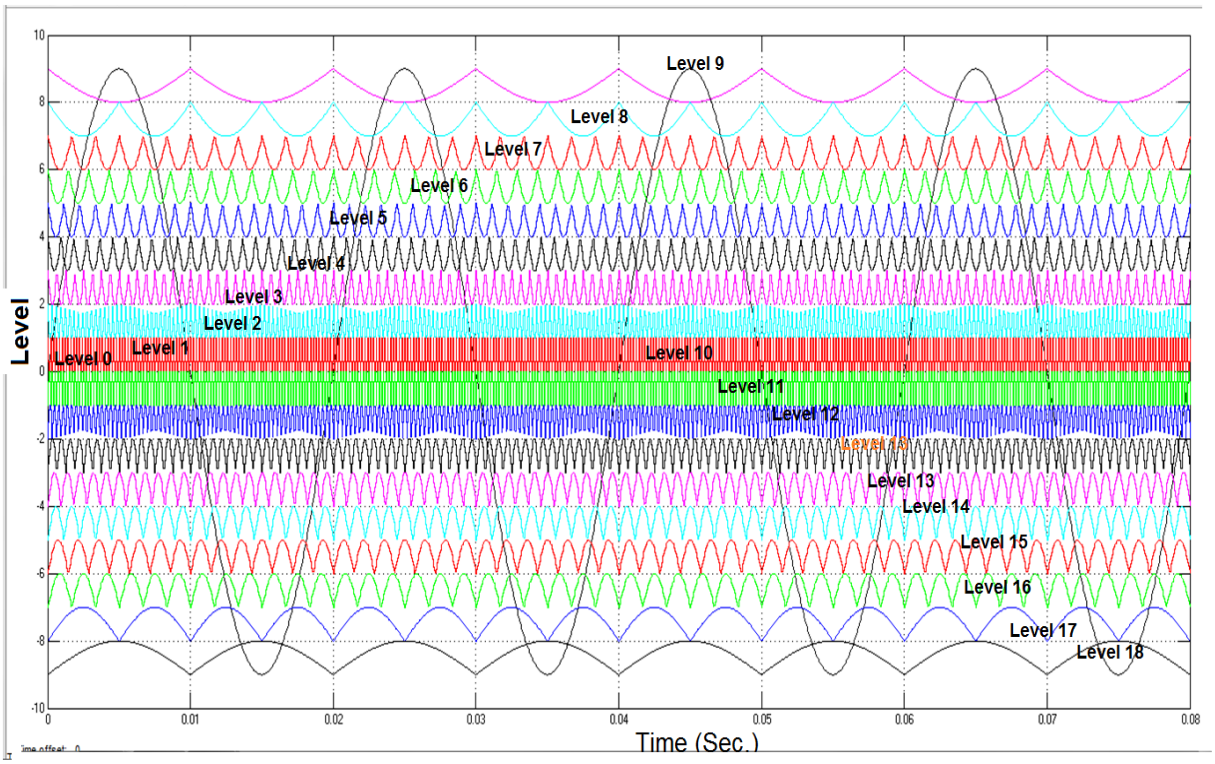


Fig 12:- Variable Frequency PWM Technique for 19 Level Inverter

➢ *Carrier Frequency for different levels*

Level	Frequency (Hz)
0	-
1	900
2	800
3	700
4	600
5	500
6	400
7	300
8	200
9	100
10	900
11	800
12	700
13	600
14	500
15	400
16	300
17	200
18	100

Table 5:- Different Carrier Frequencies for 19 Level MLI

In this way the 7 as well as 19 level MLI are analyzed and implemented with VFISPWM technique whose results are discussed in next chapter.

III.RESULTS

The Simulation Result Analysis is done on model by running a simulation. MATLAB Simulation model of 7 level MLI using PDPWM, POPWM, APODPWM, VFISPWM technique of inverters are discussed in previous chapter and performance results are given below

➢ *Phase Diposition*

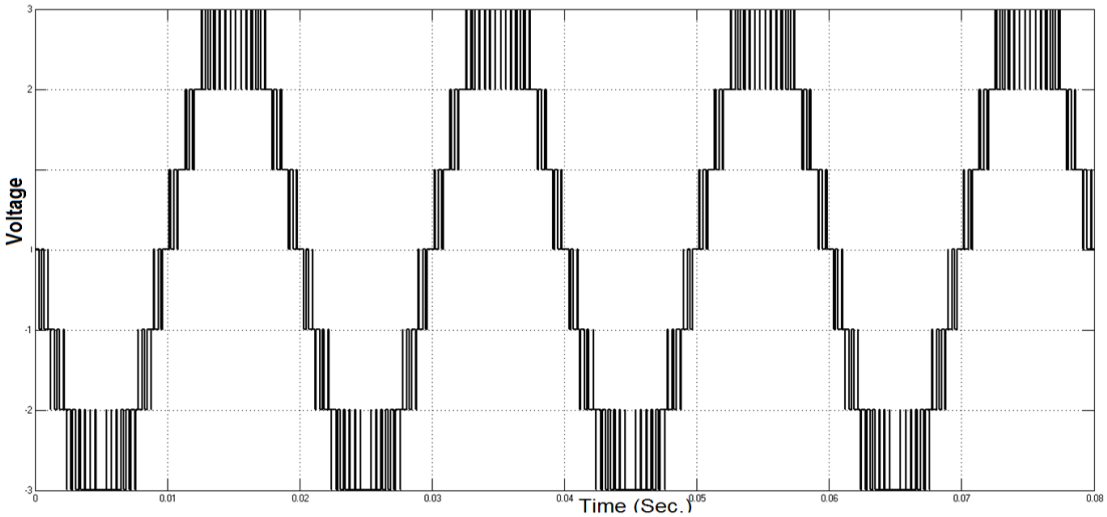


Fig 13:- Output Voltage of Seven Level MLI using POPWM

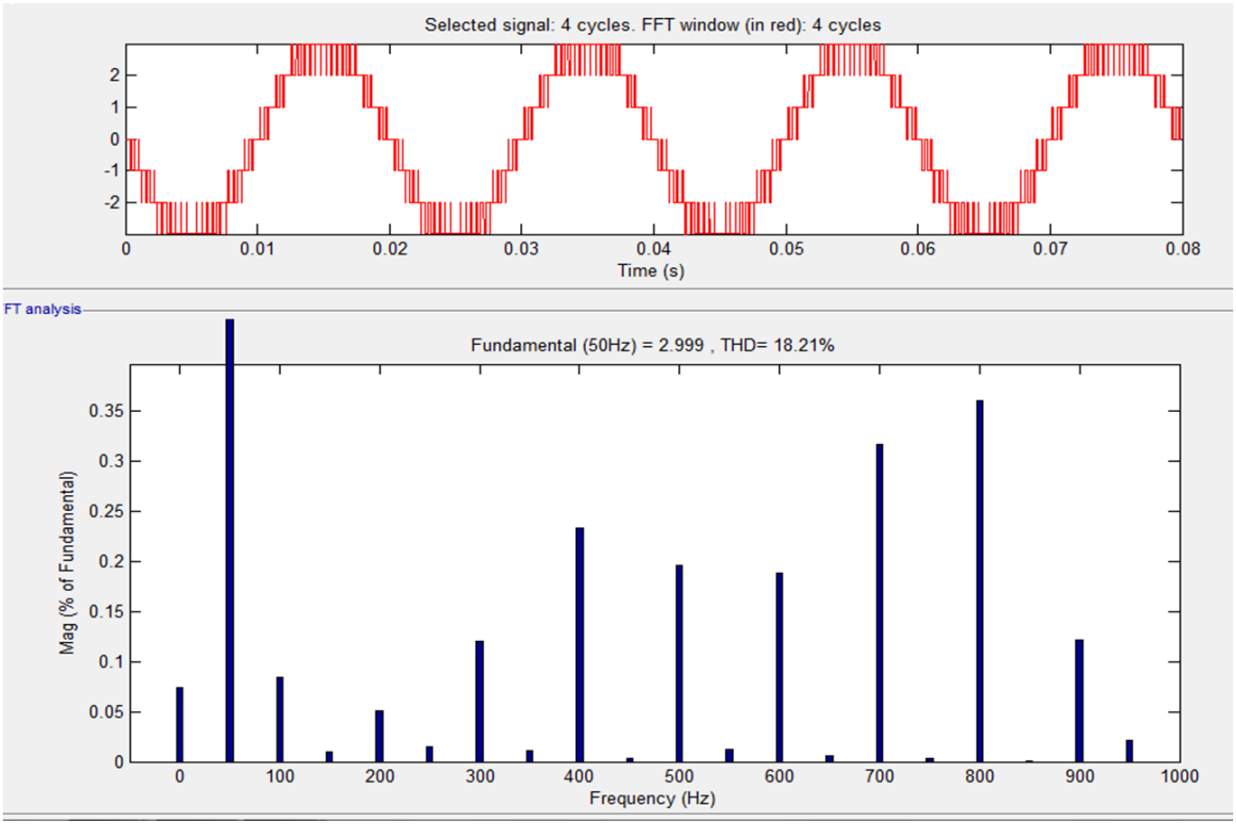


Fig 14:- FFT Analysis of Seven Level PDPWM

➢ *Phase Opposition*

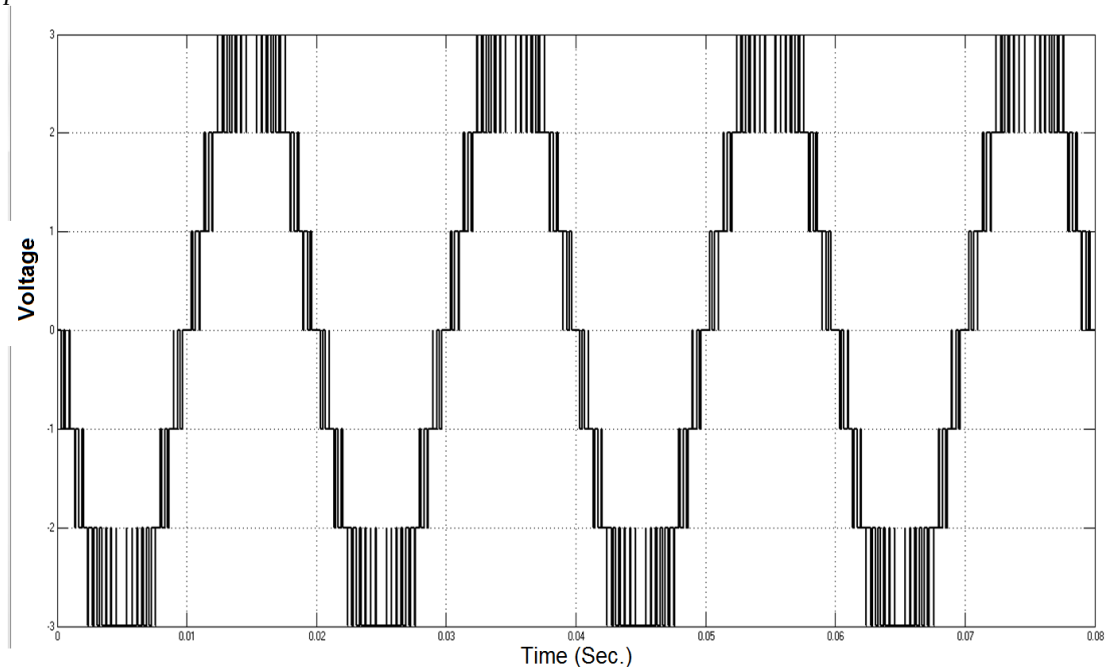


Fig 15:- Output Voltage of Seven Level MLI using POPWM

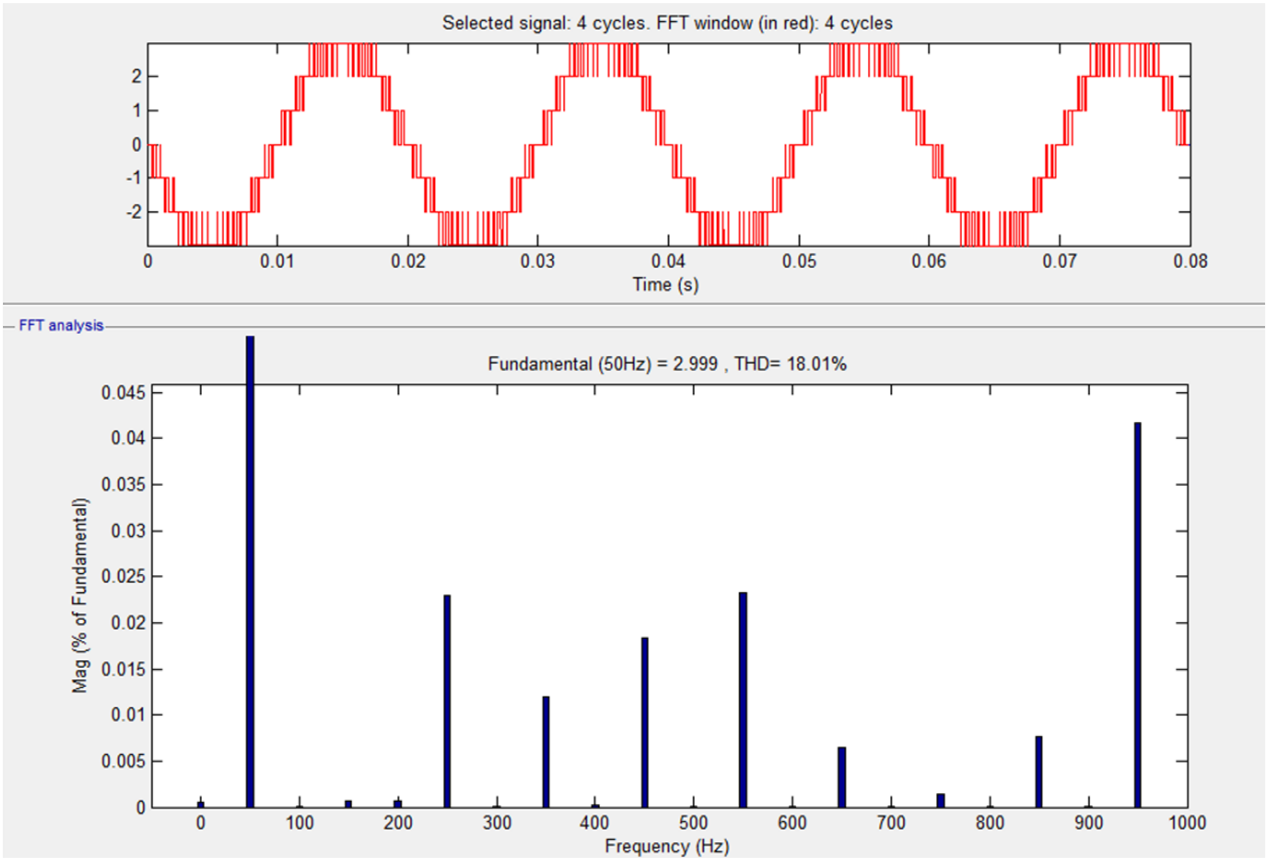


Fig 16:- FFT Analysis of Seven Level POPWM

➢ *Alternate Phase Opposition Diposition*

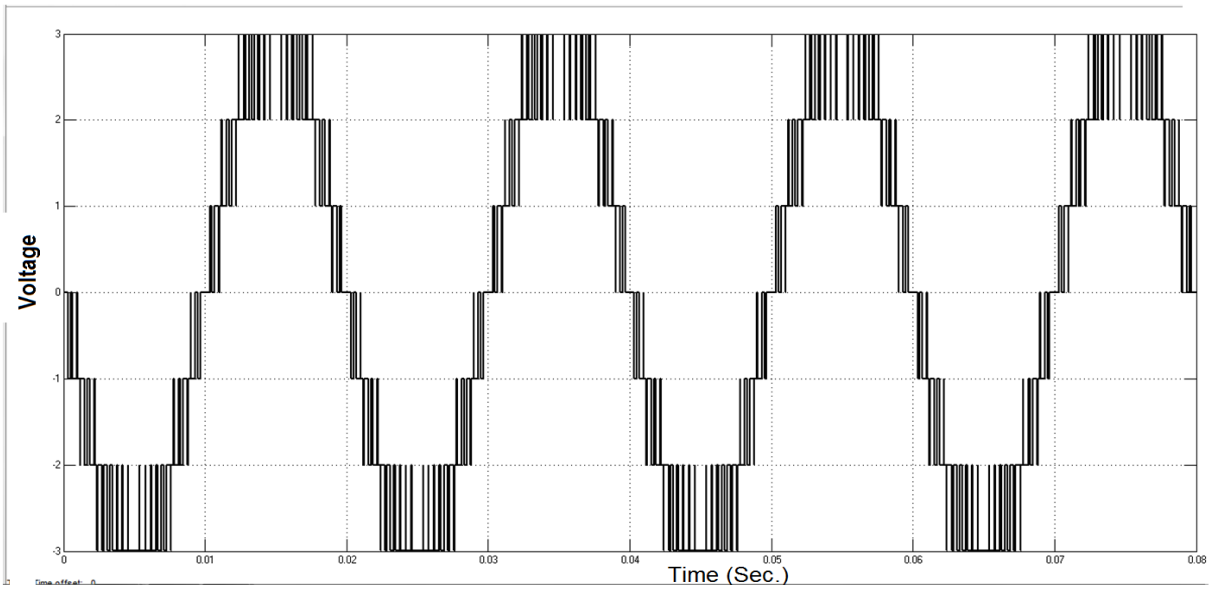


Fig 17:- Output Voltage of Seven Level MLI using APODPWM

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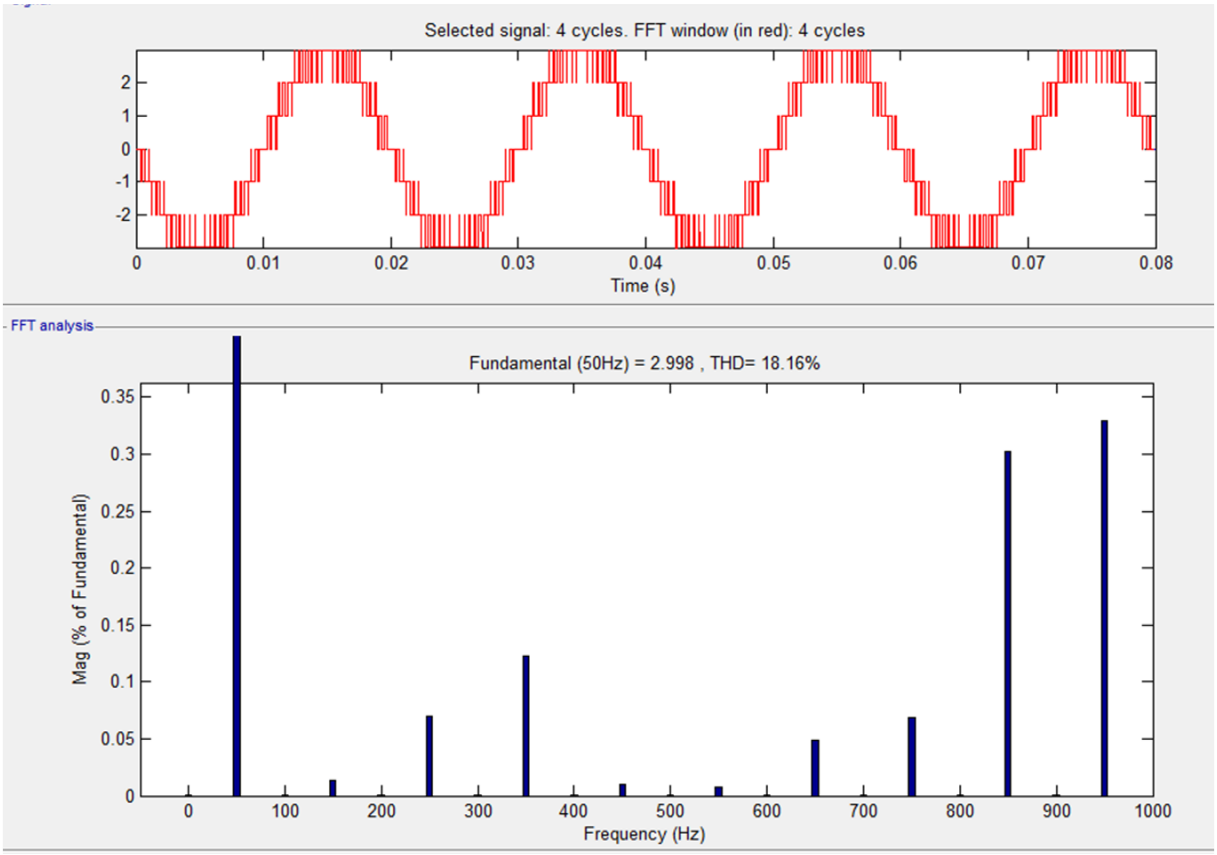

Fig 18:- FFT Analysis of Seven Level APODPWM

➢ *VFISC-PWM*

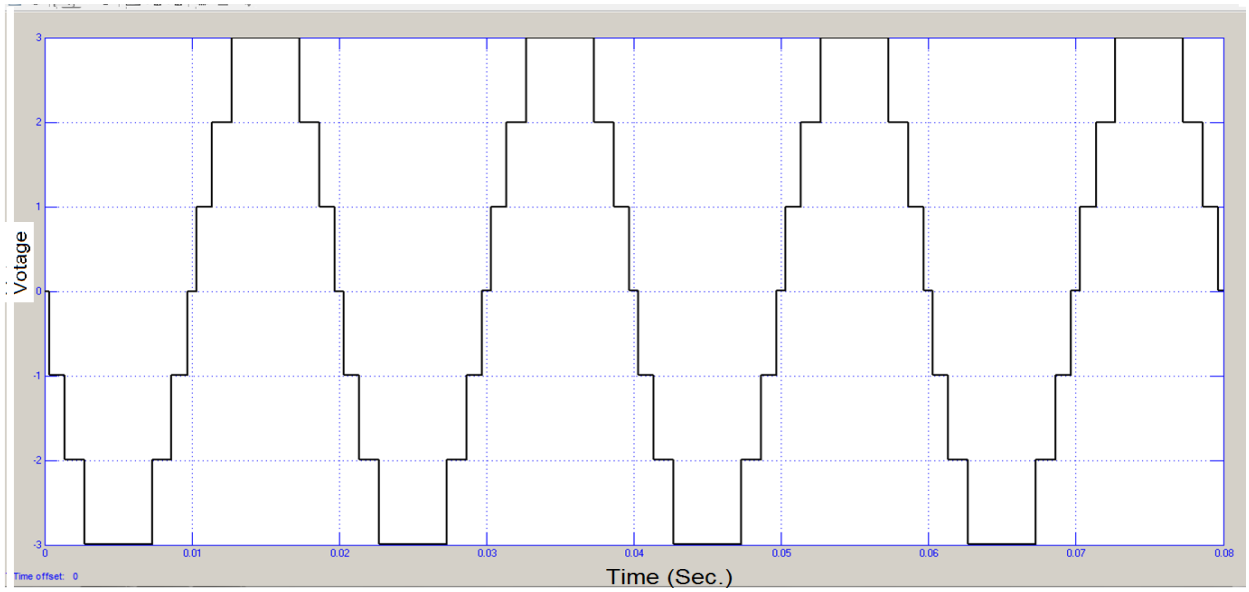

Fig 19:- Output Voltage of Seven Level MLI using VFISPWM

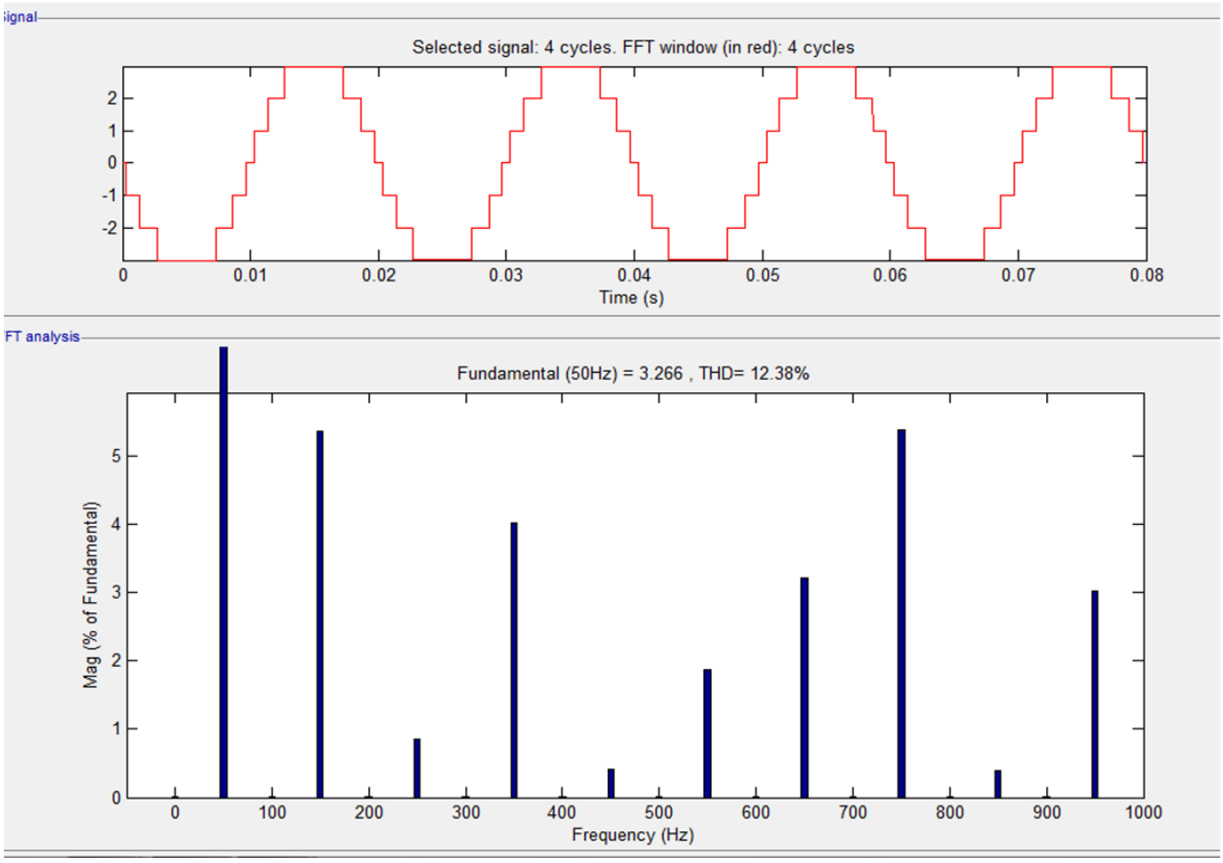

Fig 20:- FFT Analysis of Seven Level VFISPWM

➢ *For 19 Level MLI*

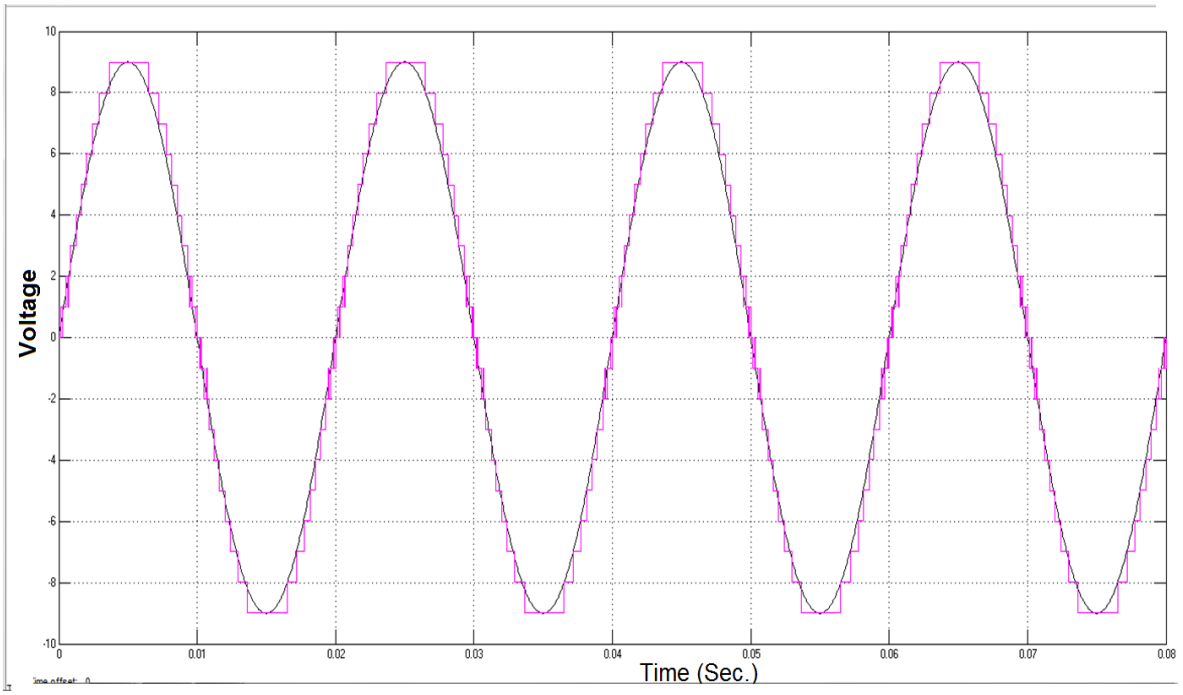

Fig 21:- Output Voltage of Ninteen Level MLI using VFISPWM

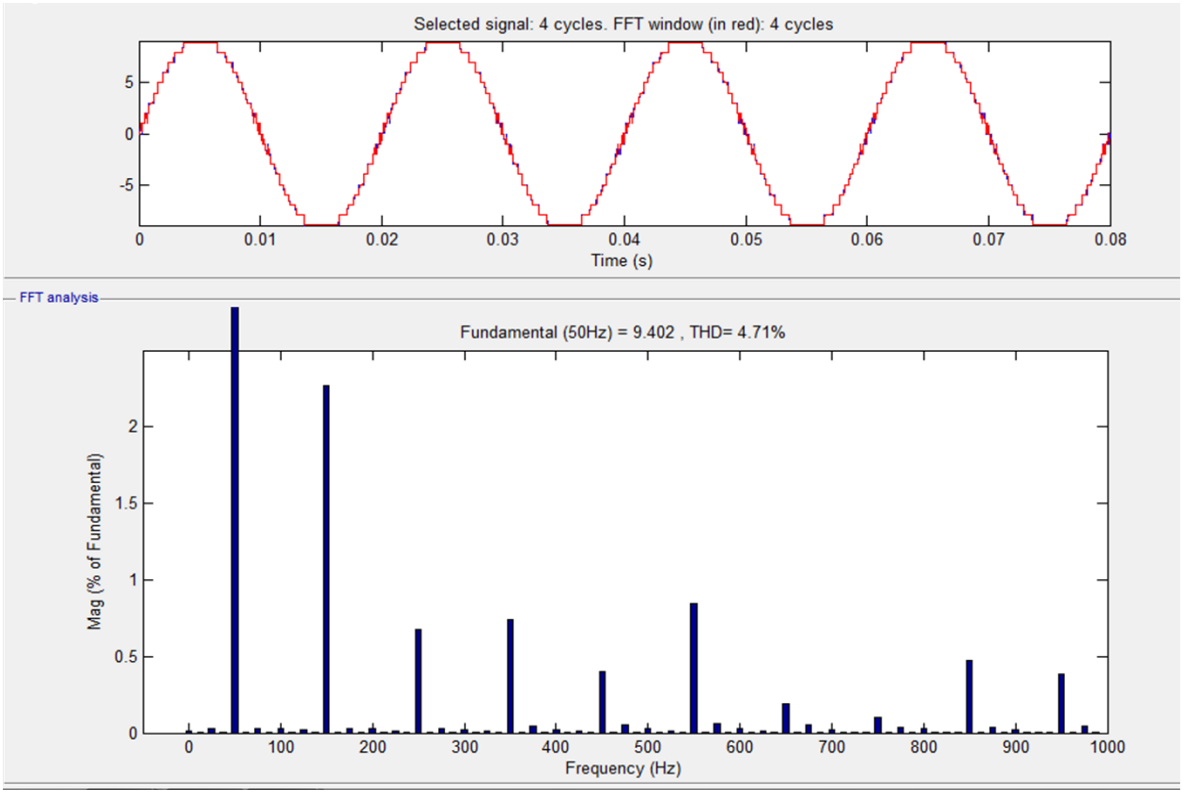

Fig 22:- FFT Analysis of Nineteen Level VFISPWM

➢ *THD Comparison Table : for different MLI & PWM Techniques*

MLI Level	PWM Technique	THD (%)
7 Level	**PDPWM**	**18.21**
7 Level	**PODPWM**	**18.01**
7 Level	**APODPWM**	**18.16**
7 Level	**VFIS PWM**	**12.38**
19 Level	**VFIS PWM**	**4.71**

Table 6: THD of different MLI & PWM Techniques

The output waveform and simulation results along with total harmonic distortion for 7 level inverter is shown in figure 19

IV. CONCLUSION

The switches requirement for 7 level and 19 level asymmetrical inverter are 8 and 12 respectively which are very less as compared to all three symmetrical topologies [6] and thus increased the compactness and the complexity size along with cost of multilevel inverter reduces also from figure 4 and figure 5 we can conclude the harmonic distortion reduces to greater extent in case if 19 level inverter as compared to 7 level inverter with proposed topology.

REFERENCES

[1]. Y. Suresh Anup Kumar Panda "Investigation on hybrid cascaded multilevel inverter with reduced dc sources" Renewable and Sustainable Energy Reviews 26 (2013) 49–59.
[2]. J. Rodriguez, J. S. Lai and F. Z. Peng, "Multilevel Inverters: Survey of Topologies, Controls, and Applications," IEEETransactions on Industry Applications, vol. 49, no. 4, Aug. 2002, pp. 724-738.
[3]. J. S. Lai and F. Z. Peng, "Multilevel Converters-A new Breed of Power Converters," IEEE Trans. Ind. Applications.,vol.32,pp. 509-517, May/June 1996.
[4]. Gupta, K.K.; Jain, S.; , "Topology for multilevel inverters to attain maximum number of levels from given DC sources," Power Electronics, IET , vol.5, no.4, pp.435-446, April 2012.
[5]. HEMA LATHA JAVVAJI, B. BASAVARAJA "Simulation & Analysis of Different Parameters of Various Levels of Cascaded H Bridge Multilevel Inverter" 2013 IEEE Asia Pacific Conference on

Postgraduate Research in Microelectronics and Electronics (PrimeAsia).
[6]. Anjali Krishna R , L Padma Suresh , "A Brief Review on Multi Level Inverter Topologies,"2016 International Conference on Circuit, Power and Computing Technologies [ICCPCT].
[7]. Kalpani Thantirige, Akshay Kumar Rathore, Sanjib Kumar Panda, Suvajit Mukherjee, Michael A. Zagrodnik, Amit Kumar Gupta, "An Open-switch Fault Detection Method for Cascaded H-Bridge Multilevel Inverter fed Industrial Drives,"2016 IEEE conference.
[8]. Tanmay Shukla, Priyavand bundela," Proposed Topology For Multi Level Inverter: A Review"ijisrt (International Journal of Innovative Science and Research Technology) Volume 3, Issue 9, September – 2018