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Study on Intel 80386 Microprocessor

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Abstract:- 80386 Microprocessor is one of the major type of microprocessor in x86 series of Intel. This paper deals speaks about the detailed description of 80386 Microprocessor like its architecture, registers…etc.

Keywords:- *Architecture, Flag Registers, Memory Management…etc*.

I. INTRODUCTION

1. Another name of Intel 80386 is *386 or i386* is one of the microprocessor in third-generation Intel x86 series.
2. 80386 were developed by Intel in October 1985.
3. The 386 microprocessor processor roughly followed Intel's 8086 and 80286 processor and predated the 80486.
4. 11 million instructions per second (MIPS) can be stored using 80386.
5. Its features are:

- Protected mode capabilities
- Contain instruction set and 32-bit registers .
- Virtual memory support using paging translation unit.
- Speeds ranges from 12 MHz to 40 MHz.
- Memory support up to 4GB.

II. ARCHITECTURE

1. The Internal Architecture of 80386 is classified into 3 sections.

➢ *Central Processing Unit(CPU)*
➢ *Memory Management Unit(MMU)*
➢ *Bus Interface Unit(BIU)*

2. The first unit, CPU is again divided into two

➢ *Execution unit*
➢ *Instruction unit*

3. The Execution unit of CPU has *8 General purpose registers and 8 Special purpose registers* which can be used to calculate offset address and can handle data.
4. With the help of Instruction unit, CPU decodes the opcode bytes received from the 16-byte instruction code queue and it arranges the results into a 3- instruction decoded queue.
5. After decoding the instructions, the next step is to pass the decoded instruction into the control section for deriving the necessary control signals for the instruction to be decoded. The **barrel shifter** is used to increase the speed of all shifts and rotate operations in the instruction.
6. In order to complete the operations in minimum time, we can implements the bit-shift-rotate algorithms to use multiply / divide logic.
7. With the help of multiply or divide logic, 32- bit multiplications can be executed within one microsecond.
8. Next unit of 80386 is Memory management unit or simply MMU consists of

- *Segmentation unit*
- *Paging unit.*

9. Two address components of Segmentation unit *segment and offset* helps for revocability and sharing of code and data.
10. The maximum size of Segmentation unit is 4GB.
11. Using paging unit, the physical memory is partitioned into fixed size pages of 4KB size.
12. The superior of paging Unit is the Segmentation unit which works under the control of the Segmentation Unit. It means, each segment is again divided into fixed sized pages. Using the Memory Management Unit(MMU) , the virtual memory also called illusion memory which organized its space into segments and pages
13. 4 level protection mechanism of Segmentation unit, which offers the protecting and isolating system code and also offers data from the application program.
14. Conversion of linear addresses into physical addresses is carried out by paging unit.
15. The page level privileges are checked with the help of PLA attribute.
16. Every page maintains the paging information of the task which is performed. To avoid invalid conditions, PLA checks segment limits and attributes at segment level accesses code and also checks to the data in the memory segments.
17. The last section of 80386 is the Bus Interface Unit or BIU has a capacity to prioritize various bus requests. Bus control access is handled with the BIU. The address signal from A0-A31 of address driver which drives the bus enable signal and address signal. Related control signals are handled using the pipeline and dynamic bus sizing unit.
18. Finally, interface with the internal data bus and system bus is done with Data Buffers.

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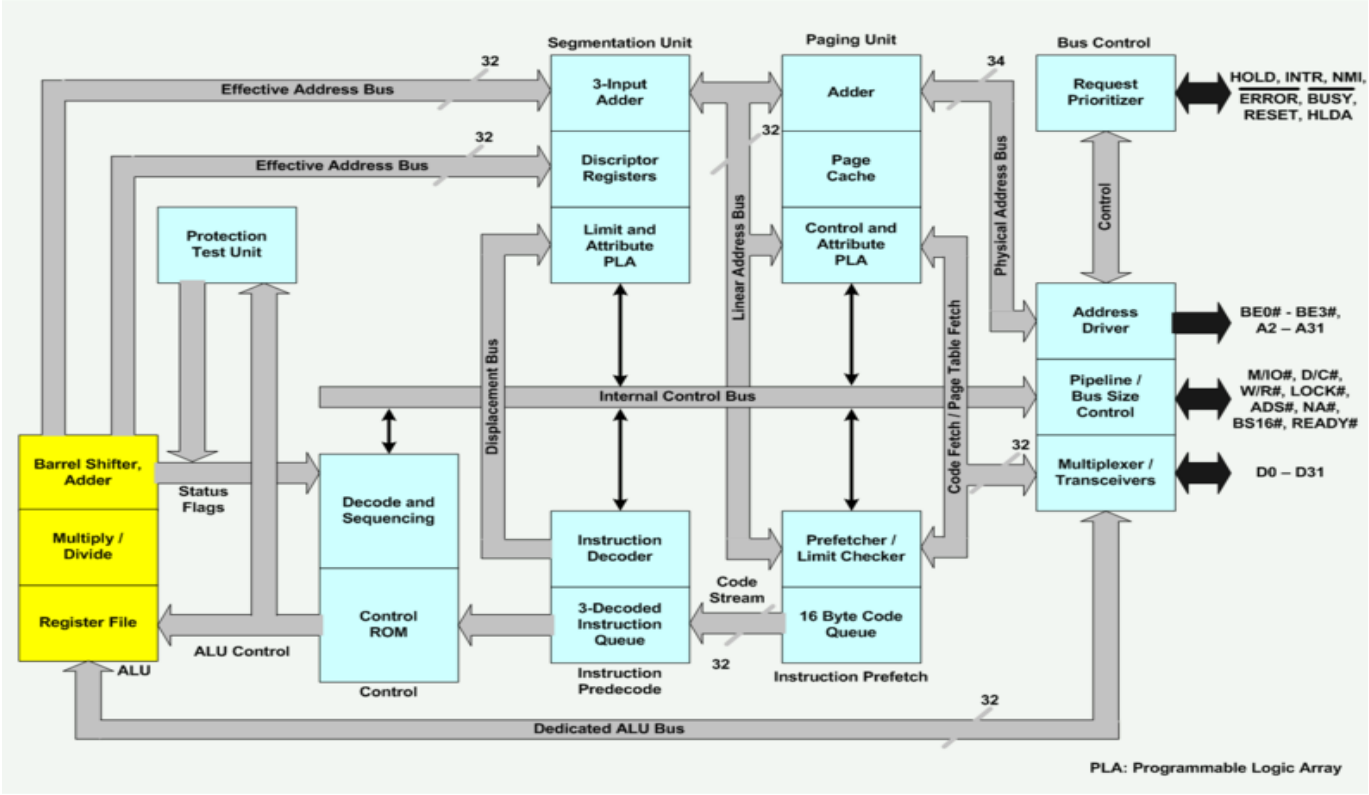

Fig 1

III. FLAG REGISTERS OF 80386

1. 80386 Microprocessor uses the Flag register of 32 bit size.
2. 16 bit of this flag is functionally similar to 8086 and 80286 microprocessor. The additional flags are discussed below.
3. The reserved bits of intel microprocessor are D18 - D31, D5 and D3 from out of these 32 bits. D1 is always set at 1.
4. In order to derive the flag register of 80386, two extra new flags are added to the 80286 flag. They are VM flag and flag RF flag.
5. *Virtual Mode Flag (VM):* If VM = 1, the 80386 is get into virtual mode of within the protection mode. The VM flag is only set when the 80386 is in protected mode. In this VM mode, an exception 13 is generated if any privileged instruction is executed.
6. *Resume Flag (RF):* RF flag is used with the collaboration of debug register breakpoints. In the start point of each and every instruction cycle, the flag is checked and if RF=1, and any debug fault occur it automatically ignored the fault during the instruction cycle. After the successful execution of every instruction, the RF flag is automatically reset.
7. The RF flag is not automatically cleared after the successful execution of CALL, JMP and INT instruction which cause a task switch. The above instructions are used to set the RF to the value specified by the memory data available at the stack.

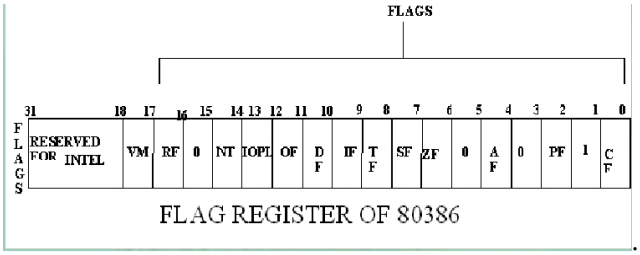

Fig 2

IV. GENERAL PURPOSE REGISTERS

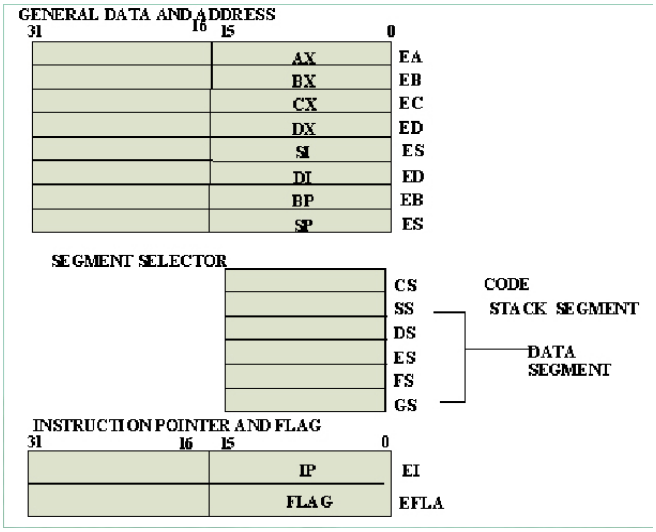

Fig 3

V. FEATURES OF 80386

1. 80386 supports 8 or 16 or 32 bit data operands
2. Compared to other x86 families 80386 has 132 pins.
3. It has a strong 32-bit internal registers which supports 32-bit data bus and 32-bit non-multiplexed address bus
4. The Physical Address of 8086 is 4GB with Maximum Segment size of 4GB and Virtual Address of 64TB(4GB seg. * 16,384 segments)
5. 3 variations of 80386

A. **80386DX** supports floating point capability
B. **80386SX** have16-bit data bus
C. **80386SL** contains several power management options

6. 3 different modes of operations are;

A. Real Mode
B. Protected Mode
C. Virtual Mode

7. Memory Management Unit or MMU provides paging , virtual memory and 4 levels of protection. it is low power consumption & Low cost.
8. The Clock Frequency ranges are20,25 and 33MHz

V. MEMORY SYSTEM

1. The physical **memory** of an **80386 system** is organized as a sequence of 8-bit bytes.
2. Each byte is assigned a unique address that ranges from zero to a maximum of 2^ (32) -1 (4 gigabytes).
3. **80386** programs, however, are independent of the physical address space.
4. The memory management unit has two separate units within it. These are

- **Segmentation Unit**
- **Paging Unit**

5. **Segmentation unit**:. It offers protection mechanism in order to protect the code or data present in the memory from application programs.
6. It gives **4 level protections** to the data or code present in the memory.
7. Every information in the memory is assigned a privilege level from PL0 to PL3. Here, ***PL0 holds the highest priority*** and PL3 holds the lowest priority.
8. **Paging unit:** supports multitasking. This is so because the physical memory is not required to hold the whole segment of any task. Despite, only that part of the segment which is needed to be currently executed must be stored in that memory whose physical address is calculated by the paging unit,

VI. SUMMARY

1. 80386 is a 32bit processor that supports 8bit/32bit data operands.
2. 80386 instruction set is upward compatible with all its predecessors.
3. The memory management section of 80386 supports the virtual memory, paging and four levels of protection, maintaining full compatibility with 80286.
4. For mathematical data processing, the 80386 microprocessor can be supported by 80387.
5. 80386 can run 8086 applications under protected mode in its virtual 8086 mode of Operation.

REFERENCES

[1]. Intel 80386 Programmer's Reference Manual 1986
[2]. Text book:*The Intel Microprocessors: 8086/8088, 80186/80188, 80286, 80386, 80486, Pentium, Pentium Pro Processor, Pentium II, Pentium III, Pentium 4 and Core2 with 64 - bit Extensions*