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A Novel 9-Level Switched Capacitor Inverter Using Different Carrier Based PWM Techniques

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Abstract:- In this paper, a new 9-level inverter employing switched capacitor technique is proposed. Three bidirectional voltage blocking switches are employed to connect the four H-bridges and to incorporate the three switched capacitors. The proposed multilevel inverter (MLI) circuit outputs a 9-level waveform with a maximum boosting factor of four. Unlike the already established switched capacitor based MLI consisting of two stages the proposed MLI is single stage inverter. The switches in the proposed MLI is subjected to a low value of voltage stress equal to V_{dc}. The proposed MLI is further analyzed by using various multicarrier sinusoidal PWM technique such as Phase Shift PWM (PSPWM), Phase disposition PWM (PDPWM), Phase Opposition Disposition PWM (PODPWM), Alternate Phase Opposition Disposition PWM (APODPWM) and Variable Frequency PWM (VFPWM).

Keywords:- *Multilevel inverter, boosting-factor, Switched-Capacitor (SC), PDPWM, PODPWM, APODPWM, VFPWM, COPWM, PSPWM.*

I. INTRODUCTION

The use of conventional energy sources and its impact on our environment had led researchers and governments to shift their focus on using non-conventional sources of energy such as hydro energy, solar energy and wind energy for meeting our energy requirement. A number of different power converters has been employed to act as an interface between these new energy systems and electric grid. One such converter employed is a multi-level inverter that plays a crucial role of converting DC power to AC power.

The first multilevel inverter topology was introduced in 1970s and was proposed by Baker et al [1]. The idea for multilevel inverters was proposed to overcome the problems associated with the traditional two-level inverter. The three basic multilevel inverter topologies are the neutral point clamped [2], flying capacitor [3]and cascaded H-bridge converter [4]. These multilevel inverters have been playing a crucial role in different high-end industrial applications. These multilevel inverters suffered from various limitations such as high voltage stress across the switching devices, the use of multiple isolated DC sources and increased device account as the number of output level increases. Also, voltage boosting factor for these traditional inverters is confined to one

To address the issues of low voltage boosting factor, the concept of charge pump employing switched capacitor had been used recently [5]. A charge pump can output a voltage higher than its input voltage. Whenever the capacitor is connected across the source it gets charged and when connected in series to the source the capacitor starts discharging transferring the stored energy to the load. Multilevel inverters employing switched capacitor technique has been proposed in [6] [7] [8] .The topologies presented in these papers consisted of two a stage configuration. The topology presented in [6] consist of dc-dc multilevel converter cascaded to an H-bridge. The dc-dc converter produces the required positive voltage levels and is known as the level generation side and the H-bridge act as the polarity generation side producing the required bipolar waveform. A major shortcoming of the above said topologies is that the semiconductor switches in the polarity generation side has to suffer from high voltage stress.

To overcome the limitation of high voltage stress in the above said topologies, a new MLI topology employing switched capacitor has been presented in [9]. The topology in [9] is a single stage switched capacitor topology made up of three cascaded H-bridges. This topology reduces the voltage stress across switching devices to a low value equal to the input dc source.

This paper proposes a new 9-level switched capacitor based MLI with a voltage boosting factor of 4. The proposed multilevel circuit is further analyzed using different PWM techniques such as PDPWM, PODPWM, APODPWM, VFPWM and PSPWM. The proposed topology has two important merits, firstly it is able to produce a maximum output voltage of $4V_{dc}$ i.e. the circuit is able to produce a voltage boosting factor of four, secondly, the switches suffers from a low value of voltage stress.

This paper is categorized in the following manner: section II, consists of circuit analysis and operation of the new 9-level inverter. Section III, discuss about various carrier based PWM technique employed in this paper. Section IV, consists of results of various MATLAB simulations. Finally, section V deduces a conclusion.

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II. CIRCUIT ANALYSIS AND SWITCHING STATES

The proposed 9-level MLI circuit is shown in Fig.1. The circuit consists of four H-bridge, the neutral point of each H-bridges is connected via three bidirectional voltage blocking switches. The bidirectional voltage blocking switch is made up of two MOSFETs switches connected back to back. To make use of the charge pump technique 3-floating capacitors namely C_1, C_2, & C_3 are being employed in the circuit. The capacitor C_1, C_2 & C_3 gets charged when connected across the dc input source and when connected in series to the source they get discharged thereby transferring their stored energy to the load. The charge pump technique employing switched capacitors allow the circuit to produce a peak output voltage of $4V_{dc}$ with just one dc source.

The topologies discussed in [6] [7] [8] had a major shortcoming i.e., the power semiconductor switches in the polarity generation side has to suffer from a high voltage stress. However, for the switched capacitor inverter proposed in this paper the maximum voltage stress is limited a low value equal to V_{dc}. Thus, the proposed inverter can be constructed by making use of switches that are of low voltage rating. To effectively validate the fact that the switches suffer from low voltage stress equivalent circuit diagram representing all 9-voltage states is depicted in Fig.2. Equivalent states are further described in Table I.

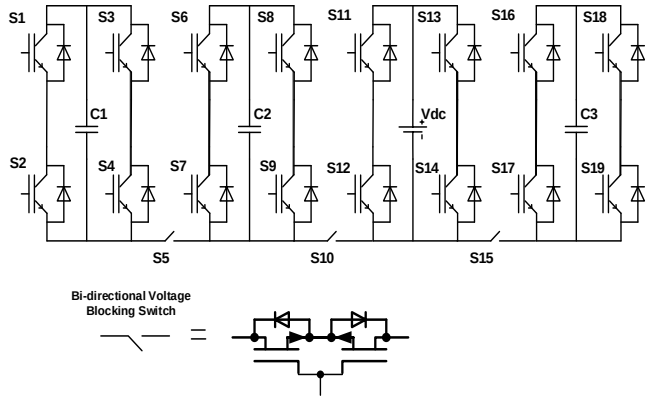
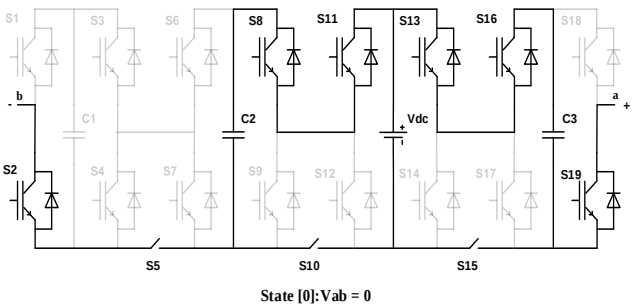
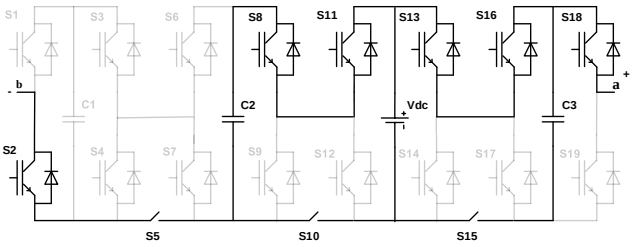


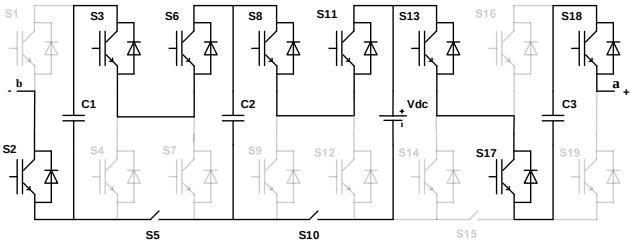
Fig 1:- Circuit diagram of the new single phase 9-level switched capacitor multilevel inverter



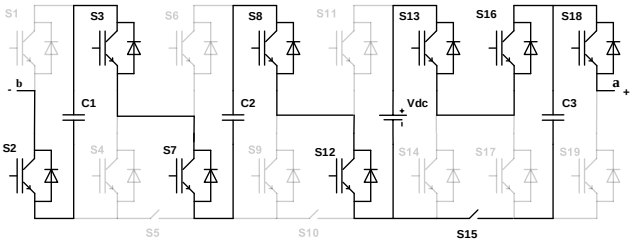
State [0]:Vab = 0



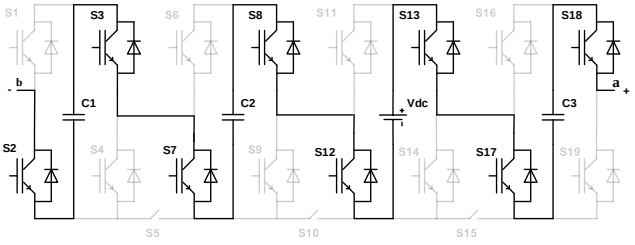
State [+1]:Vab = +1Vdc



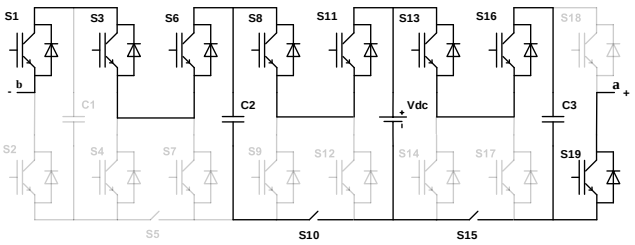
State [+2]:Vab = +2Vdc



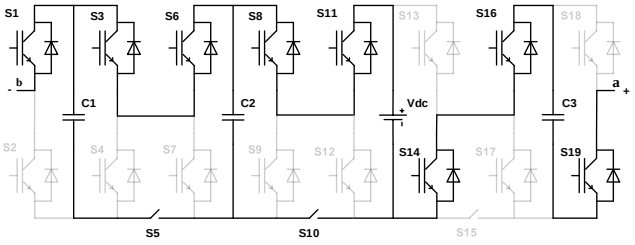
State [+3]:Vab = +3Vdc



State [+4]:Vab = +4Vdc



State [-1]:Vab = -1Vdc



State [-2]:Vab = -2Vdc

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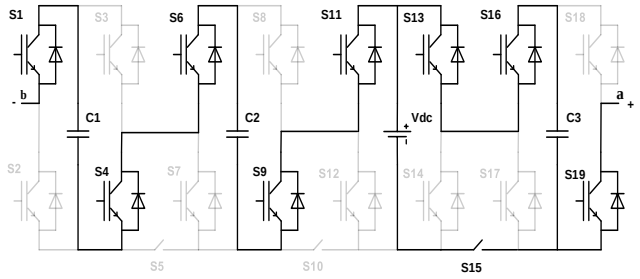
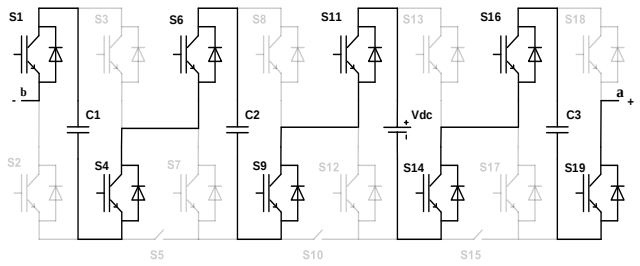


State [-3]:Vab = -3Vdc



State [-4]:Vab = -4Vdc

Fig 2:- Equivalent circuit representation for all voltage levels

Switches	STATES								
	0	+1	+2	+3	+4	-1	-2	-3	-4
S1	off	off	off	off	off	on	on	on	on
S2	on	on	on	on	on	off	off	off	off
S3	off	off	on	on	on	on	on	off	off
S4	off	off	off	off	off	off	off	on	on
S5	on	on	on	off	off	off	on	off	off
S6	off	off	on	off	off	on	on	on	on
S7	off	off	off	on	on	off	off	off	off
S8	on	on	on	on	on	on	on	off	off
S9	off	off	off	off	off	off	off	on	on
S10	on	on	on	off	off	on	on	off	off
S11	on	on	on	off	off	on	on	on	On
S12	off	off	off	on	on	off	off	off	off
S13	on	on	on	on	on	on	off	on	off
S14	off	off	off	off	off	off	on	off	on
S15	on	on	off	on	off	on	off	on	off
S16	on	on	off	on	off	on	on	on	on
S17	off	off	on	off	on	off	off	off	off
S18	off	on	on	on	on	off	off	off	off
S19	on	off	off	off	off	on	on	on	on

Table 1:- Switching Condition for the New 9-Level Switched Capacitor Mli

The main merit of the proposed 9-level MLI resides in fact that it produces a high voltage boosting factor of 4. At the same time the 9-level MLI proposed in this paper uses low voltage rating switches since it suffers from low voltage stress equals to $V_{dc.}$ Even though some of the latest switched capacitor based MLI proposed recently have an advantage of low device account such as in [10] . But the fact that they suffer from very high voltage stress far outweighs there merits of low switch count.

III. MULTICARRIER PWM TECHNIQUE

In multicarrier PWM technique, switching signals are generated by comparing two signals i.e., a carrier signal is compared with a low frequency modulating signal with [11] [12]. The modulation index (M_a) which is given as the ratio of peak value of modulating signal to the peak value of carrier signal. The modulation index decides the peak value of the fundamental output voltage .For an inverter with L-levels, (L-1) carrier waves are needed.

Multicarrier PWM can be further categorized into: Level- Shift PWM and Phase-Shifted PWM. They are briefly explained below.

A. Level-Shift PWM

In Level-shift PWM scheme, all the (L-1) carrier waves have identical frequency and amplitude but are vertically shifted. For a 9-level inverter 8-carrier waves are required which are vertically arranged. They can be further categorized as

- *Phase disposition (PD):):* In this modulation scheme, all the carrier waves for the L^{th} level inverter are identical having same frequency and as well as same the phase as depicted in Fig.3.

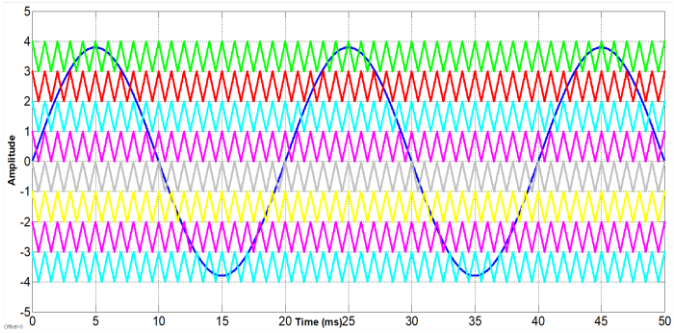


Fig 3:- PD-PWM carrier wave

- *Phase opposition disposition:* In this type of PWM technique, all the carrier waves above the above the zero refference are 180^0 out of phase with respect to the carrier waves below the zero refference as depicted in Fig.4.

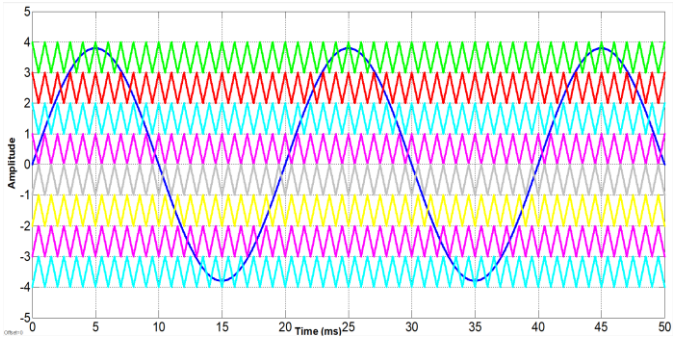


Fig 4:- POD-PWM carrier wave

- *Alternate phase opposition and disposition:* The carrier waves in this scheme are alternatively phase disposed from each other by 180^0 as depicted in Fig.5.

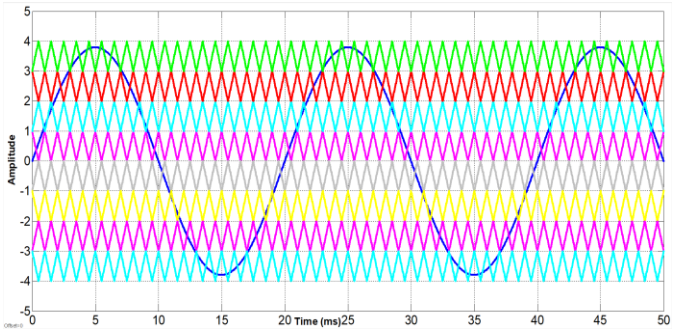


Fig 5:- APOD-PWM carrier wave

- *Variable frequency (VF):* In this scheme, the frequency of each carrier wave is different i.e., in a L^{th} level inverter the frequency of L^{th} carrier wave is greater that the (L – 1) carrier wave, this is depicted in Fig.6.

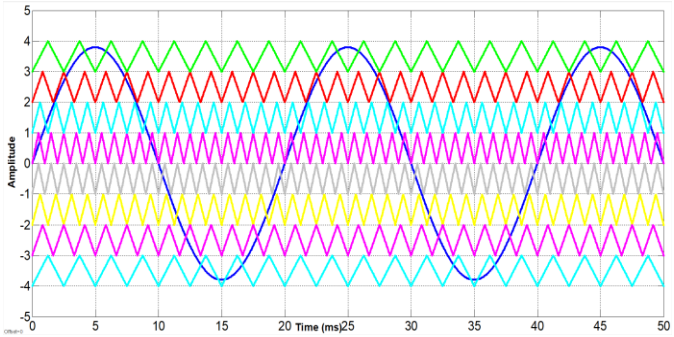


Fig 6:- VF-PWM carrier wave

B. Phase-Shifted PWM

In this PWM technique, the carrier waves for a L^{th} level inverter is phase shifted by an angle $360^0/(L-1)$ i.e., for a 9-level inverter a phase shift of 45^0 is provided between each carrier wave as depicted n Fig.7.

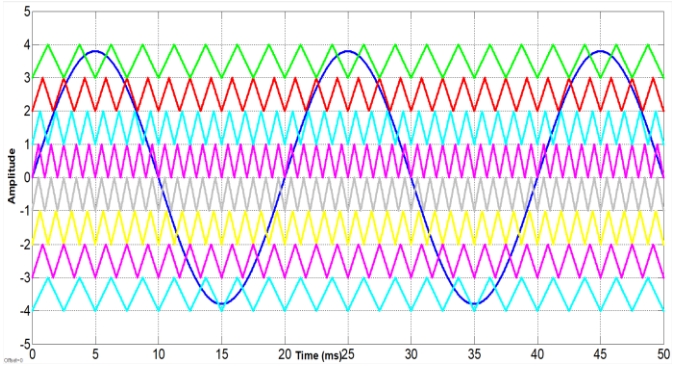


Fig 7:- PS-PWM carrier wave

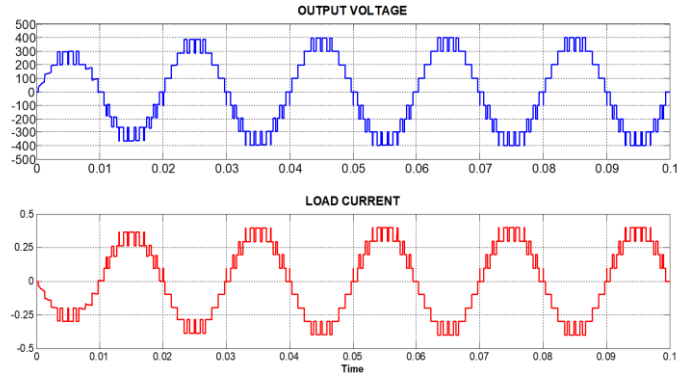
IV. SIMULATION RESULTS

The simulation of the new 9-level inverter is carried out with the help of Matlab/Simulink software. Different carrier based PWM technique are employed for generating the required output voltage and load current waveform foe a resistive load. The simulation parameter for the proposed inverter is tabulate in Table 2.

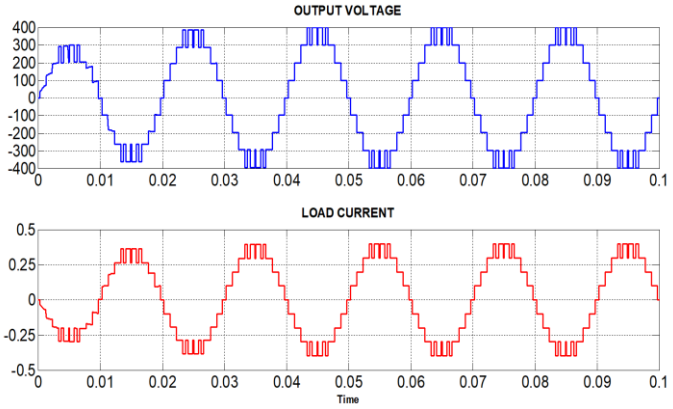
SYSTEM PARAMETER	VALUE
V_{dc}	100V
R_L	150Ω
$C_1 = C_2 = C_3 = C$	5000µF
F_C	1000Hz
F_m	50Hz

Table 2:- 9-Level Converter Parameter In Matlab

The output voltage and load current waveform for all PWM technique discussed earlier is depicted in Fig.8. FFT analysis of the new 9-level inverter using various carrier based PWM technique is performed to calculate output voltage THD at M_a=1 which is depicted in Fig.9.



(a)



(b)

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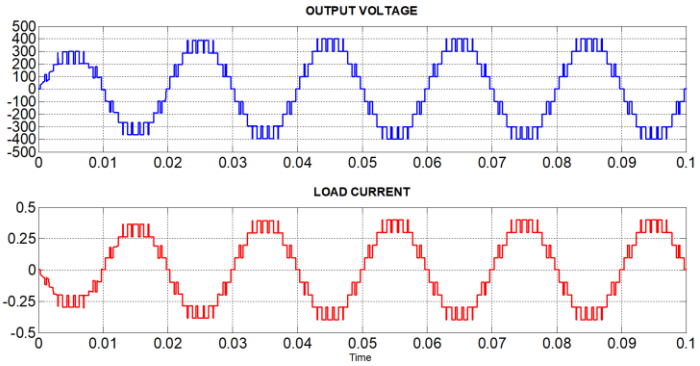

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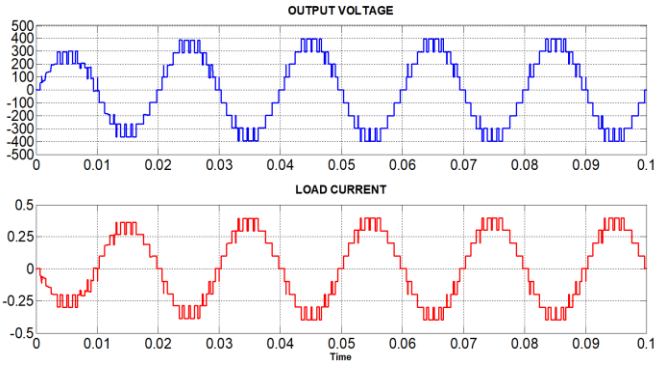
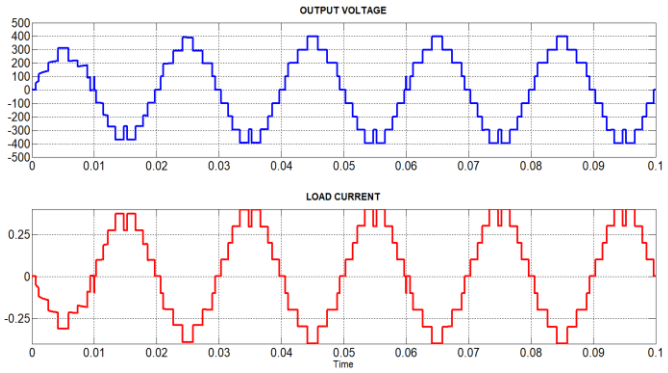


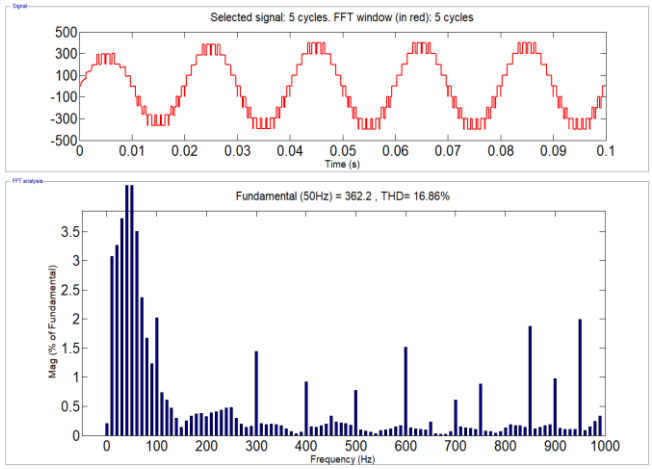
(d)



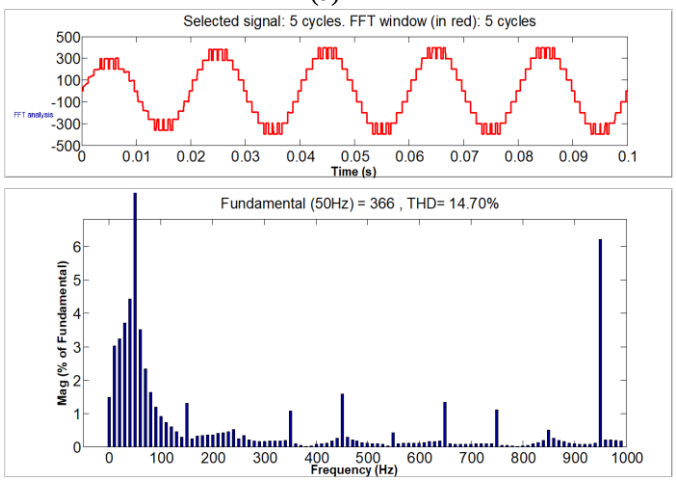
(e)

Fig 8:- Results for pure resistive load, (a) output voltage and load current waveform with PD-PWM, (b)output voltage and load current with POD-PWM, (c)output voltage and load current waveform with APOD-PWM, (d)output voltage and load current waveform with PS-PWM, (e) output voltage and load current waveform with VF-PWM.

It can also be seen that the power semiconductor switch suffers for a low value voltage stress which is identical to the value of the input voltage source. The results for THD analysis are summarized in Table 3.



(a)



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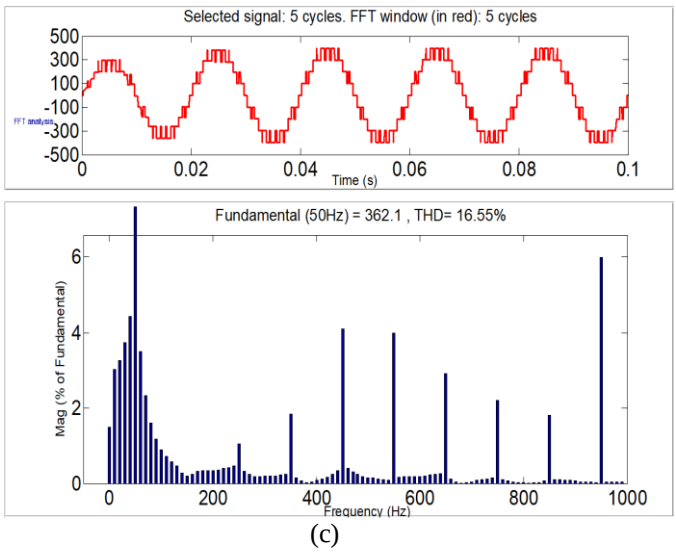

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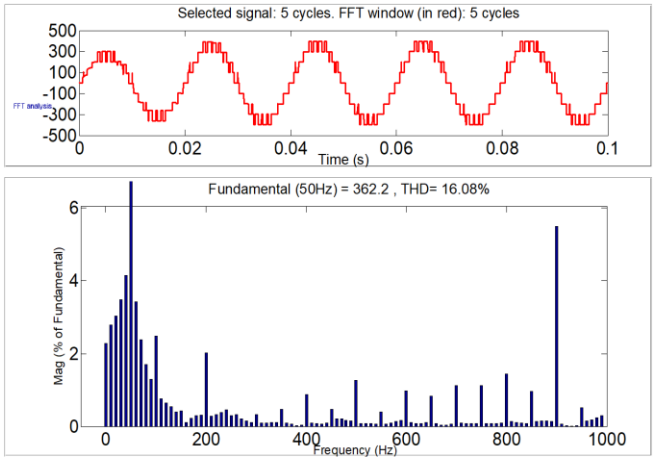

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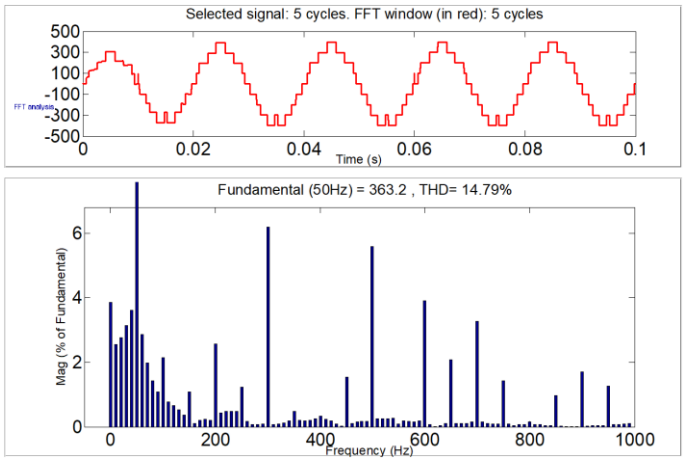

(e)

Fig 9:- Voltage THD with $m_a = 1$ (a) voltage THD for PD-PWM, (b) voltage THD for POD-PWM, (c) voltage THD for APOD-THD, (d) voltage THD for PS-PWM, (e) voltage THD for VF-THD.

$m_{a=1}$	VOLTAGE THD (%)
PD-PWM	16.86
POD-PWM	14.70
APOD-PWM	16.55
PS-PWM	16.08
VF-PWM	14.79

Table 3:- THD Analysis

It can also be seen that the power semiconductor switch suffers for a low value voltage stress which is identical to the value of the input voltage source. The results for THD analysis are summarized in Table 3.

V. CONCLUSION

A new 9-level MLI using switched capacitor technique has been presented in this paper. The proposed circuit is able to produce a 9-level waveform which has a maximum voltage, four times that of the input dc source. The proposed circuit is run using different carrier based PWM technique to further reduce the output THD. From FFT analysis it can be seen that POD-PWM technique gives us with good results when compared to other carrier based PWM technique. The fact that the 9-level circuit gives high voltage boosting factor and low voltage stress when compared to other switched capacitor circuits in its class. The new MLI inverter proposed in this paper can act as an excellent alternative for the use in single phase dc-ac conversion.

REFERENCES

[1]. H. R. Baker and H. L. Bannister, "Electric power converters," U.S Patents 3867643A, 1975.
[2]. J. Rodriguez, S. Bernet, P. k. Steimer and I. E. Lizama, "A Survey on Neutral-Point-Clamped Inverter," IEEE Transactions on Industrial Electronics, vol 57, Issue:7, pp. 2219-2230, July,2010.
[3]. M. B. Simda and F. B. Ammar, "Modellingand DBC-PSC-PWM control of a Three Phase Flaying Capacitor Stacked Multilevel Voltage Source Inverter," IEEE Transactions on Industrial Electronics, vol. 57, no. 7, pp. 2231-2239, July,2010.
[4]. M. Malinowski, K. Gopakumar, J. Rodrigues and M. A. Perez, "A Survey on Casacaded Multilevel Inverters," IEEE Transactions on Industrial Electronics, vol. 57, no. 7, pp. 2197-2206, July, 2010.
[5]. J. A. Starzyk, Y.-W. Jan and f. Qiu, "A DC-DC charge pump design based on voltage doublers," IEEE Transaction on Circuits and Systems, vol. 48, no. 3, pp. 350-359, Mar 2001.
[6]. Y. Ye, K. W. E. Cheng, J. Lui and K. Ding, "A Step-Up switched- Capacitor Multilevel Inverter With Self Voltage Balancing," IEEE Transactions on Industrial Electronics, vol. 61, no. 12, pp. 6672-6680, Dec,2014.
[7]. Y. Hinago and H. Koizumi, "A Switched-Capacitor Inverter Using Series/Parallel Conversion With Inductive Load," IEEE Transactions on Industrial Electronics, vol. 59, no. 2, pp. 878-887, Feb,2012.
[8]. J. Lui, K. Cheng and Y. Ye, "A Casacaded Multilevel Inverter Based on Switched Capacitor for High-Frequency AC Power Distribution System," IEEE Transactions on Power Electronics, vol. 29, no. 8, pp. 4219-4230, Aug,2014.
[9]. S. Lee, "A Single Phase Single Source 7-Level Inverter With Triple Voltage Boosting Gain," IEEE Access, vol. 6, pp. 30005-30011, May,2018.
[10]. R. S. Alishah, S. H. Hosseini, E. Babaei and M. Sabahi, "Optimal Design of New Cascaded Switche-Ladder Multilevel Inverter Structure," IEEE Transaction on Industrial Electronics, vol. 64, no. 3, pp. 2072-2080, March 2017.
[11]. K. Deepa, P. Kumar, V. Krishna, P. Rao, A. Mounika and D. Medhini, "A Study of Comparitive Analysis of Different PWM Techniques," in 2017 International Conference On Smart Technologies For Smart Nations, Bangalore, India, 2017.
[12]. K. Gupta and S. jain, "A Novel Universal Control Scheme for Multilevel Inverters," in 6th IET International Conference on Power Electronics, Machines and Drives, Bristol, UK, 27-29 March 2012.