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XOR Based Carry Select Adder for Area and Delay Minimization Using GDI Technology

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Abstract:- Low power and area proficient high-speed circuits are the most important areas in VLSI design research. Carry select adder is one of the fastest adders with the low area and power consumption. The paper introduces a 16-bit carry select adder with an optimized multiplexer based full adder circuit using Gate Diffusion Input logic (GDI) technology. Comparison is done on Area, Power and Delay parameters. Our circuit requires only two XOR gates and a multiplexer. In this, each logic gate is designed using GDI technology. This further reduces the transistor count resulting in Area, power, delay and complexity minimization. The proposed 16-bit carry select adder provides better results compared to the conventional 16-bit carry select adder with Area and delay.

Keywords:- *Optimized multiplexer-based adder, carry select adder, GDI technology.*

I. INTRODUCTION

The growth of high-performance processors can be upgrade by enhancing the performance of data path units. VLSI processor performance mainly depends on the type of adders used in the circuit. Any arithmetic operation can be performed using adders. Such as addition, directly by adding two numbers, Subtraction by taking the negation of subtrahend and adding to minuend, Multiplication by repeated addition, etc. Thus, Adders plays a very crucial role in designing digital integrated circuits, Microprocessors, Digital image processors, etc. Early past there are several adders like Full adder, ripple carry adder (RCA), Carry Skip Adder (CSA), Carry look-a-head adder (CLA), Carry select adder (CSLA), etc. conventional circuit of the ripple carry adder has a high propagation delay in generating outputs. To overcome this problem, a carry look-ahead adder has been designed. Here, carry propagation delay can be greatly reduced. But, the circuit becomes complex and costly as the number of variables increases. Thus, Carry Select Adder was introduced. In CSA, Ripple carry adders and multiplexers are used. So, Addition operation can be performed simultaneously in two adders by selecting carry as Cin=0 or Cin=1 through multiplexer. Thus, Circuit delay can be minimized. Though CSA is faster than any other circuit, it requires more area compared to others. To reduce area, we go with Gate Diffusion Input logic technology (GDI). GDI, a new technique of designing low power digital combinational circuits. Using this technique, Area, cost and Delay can be minimized by reducing the transistors count.

In section II, we discuss about carry select adder advantages, drawbacks and the modified circuit to overcome it. In section III, we discuss about GDI technology and implementation of modified carry select adder using GDI technology.

II. CARRY SELECT ADDER

Adder is the most frequently used digital components in the digital integrated circuit design. Carry Select Adder provides a good balance among area, cost and delay minimization. Basic blocks of CSA consist of and, or, xor gates and multiplexer. Regular carry select adder structure be made up of a pair of ripple carry adders and a multiplexer. One RCA used to evaluate, sum and carry for Cin=0 and others for evaluating the sum and carry for Cin=1. The sum and carry corresponding to Cin=0 and Cin=1 is given to the multiplexer. Based on the carry out of the previous group the sum and carry of the respective adder are selected. By making a few modifications at the gate level of carry select adder, there is still a scope of reducing area and delay. The structure of a conventional full adder and regular carry select adder is as shown in fig 1.

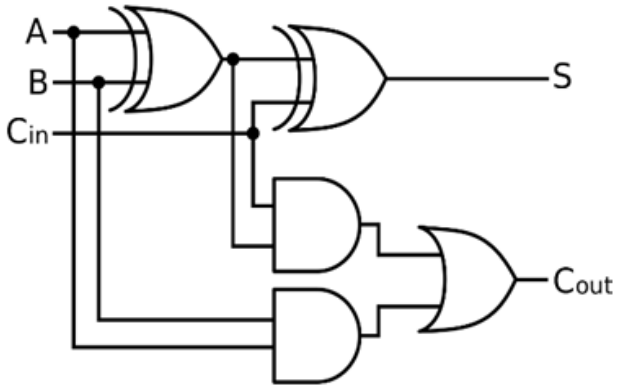

Fig 1:- Conventional Full adder

A	B	Cin	Cout	SUM
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Table 1:- Full adder – Truth table

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III. GDI TECHNOLOGY

Gate Diffusion Input logic is the latest technology in which power, area and delay get reduced. Using this technique, majority of the problem in VLSI can be minimized. In this, a greater number of transistors can be reduced compared to CMOS and RTL technologies, which further reduces the complexity and power consumption. The basic difference between GDI and other technologies is that GDI cell accommodate the inputs G, P and N. Here G is the gate input of NMOS and PMOS in common, the input to the source/drain of PMOS is P and the input to the source/drain of NMOS is N. The basic simple inverter cell has two transistors in GDI technology is given below.

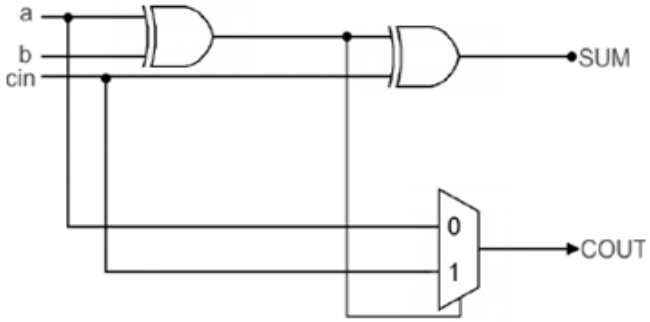


Fig 2:- Proposed Full adder

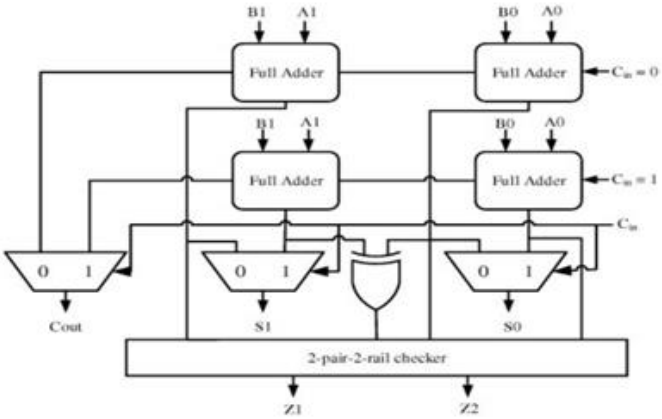


Fig 3: 2-BIT CSA (CARRY SELECT ADDER)

In GDI technology, the connected degree approach is obtainable for reducing power spending for digital circuits at the logic mode level and DC and Transient analysis of basic logic gates has been done mishandling Mod-GDI logic mode. All Simulations square measure is implemented through PSPICE supported 0.18µm CMOS technology, and results display power characteristics of GDI technique of low power digital circuit style. Simulation results shows up to 45% depletion in power-delay product in Mod-GDI. Mod-GDI approach allows realization of a broad style of many-sided logic functions by means of solely 2 transistors slighter than the semiconductor count and successively the semiconducting material space needed when it is placed after the traditional static CMOS and Domino CMOS primarily based approaches.

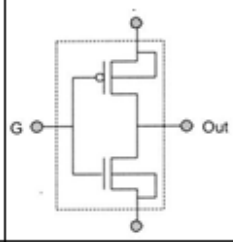
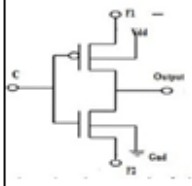
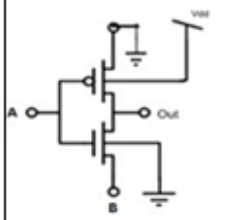
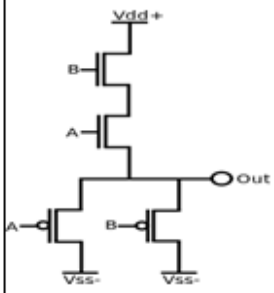
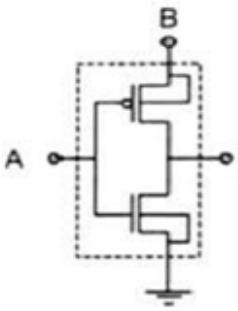
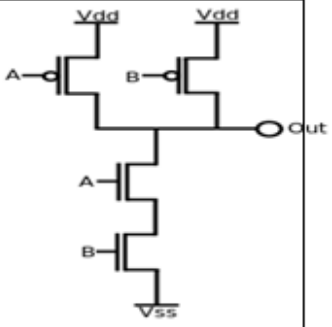
	GDI	CMOS
NOT		
AND		
OR		

Table 2:- Comparison Tables for logic gates between GDI and CMOS Technologies

If we replace all the gates in figure II using GDI technology and the full adder is constructed, then the larger area gets reduced. As full adder has 2- xor gates, 2- and gates and 1- or gate in the conventional method, it requires a total 46 transistors. Whereas in the proposed method, it reduces to 33 transistors. But using GDI technology, it reduces to 8. Delay gets reduced from 3.10 seconds to 1.45 seconds using gdi technology.

IV. PROPOSED DESIGN

The moto of this work is to reduce power supply and improve full adder's speed. During the working of the GDI methodology, by mishandling techniques like size optimizing fully adder, may leads to decrease in resource utilization. Thus results, complete carry select adder working at the one hundred rate speed with 0.75 µw power utilization. The results were obtained with Tspice simulation.

The execution of several full adders design in CMOS logic circuit and the pros and cons of each of them regarding delay, power dissipation and PDP is presented in depth. Hybrid adders are selected for the extensive evaluation. A new high performance and low power hybrid full adder was designed in 90nm Technology. The adder

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cell is classified as three modules. They are 2 - XOR gates set using 4 transistors in Gate Diffusion Input (GDI) technique and last module is carry block using GDI mux. Hybrid full adder displays low power and minimum delay. The adder improves the overall performance because of the minimum time delay. The major drawback of transmission gate logic is that it uses twice the number of transistors of the standard pass-transistor logic or more to implement the same circuit.

Implementation of 4:1 Multiplexer using GDI

A 4: 1 multiplexer comprises of 4 given input data lines as D0 to D3, S0 and S1 are 2 - select lines and Y is an output line. The output is selected among the input lines D0 to D3 based on S1 and S2 select lines.

This proposed GDI based 4:1 MUX circuit consists of the only 12T when compared to the previously proposed 46T 4:1 MUX. The number of a transistor is reduced by 36. This circuit is having the inputs, namely S0, S1, D0, D1, D2 and D3. The output is OUT.

From the logic it is observed that using the basic GDI logic, n-number of functions can be implemented. MUX design is the most complex design that can be executed with GDI, which requires only 2 transistors, whereas the traditional CMOS design requires 8 to 12 transistors.

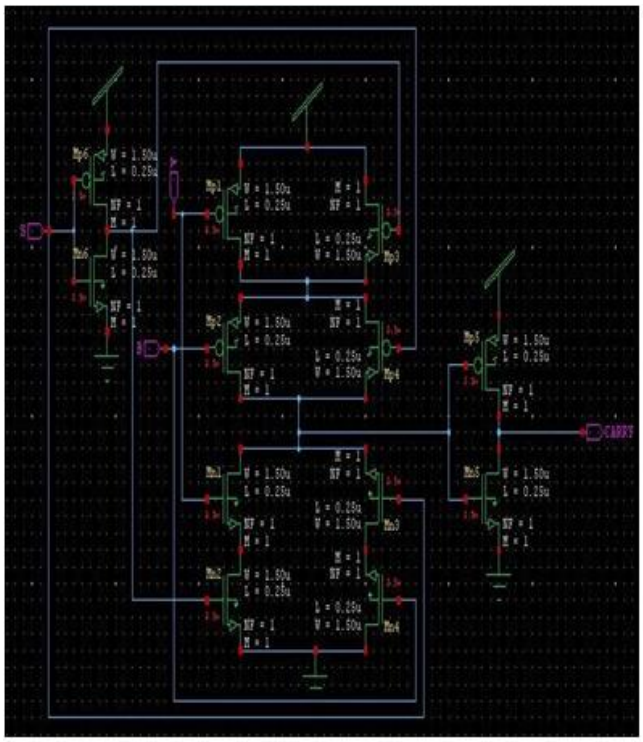

Fig 4:- CONVENTIONAL MUX

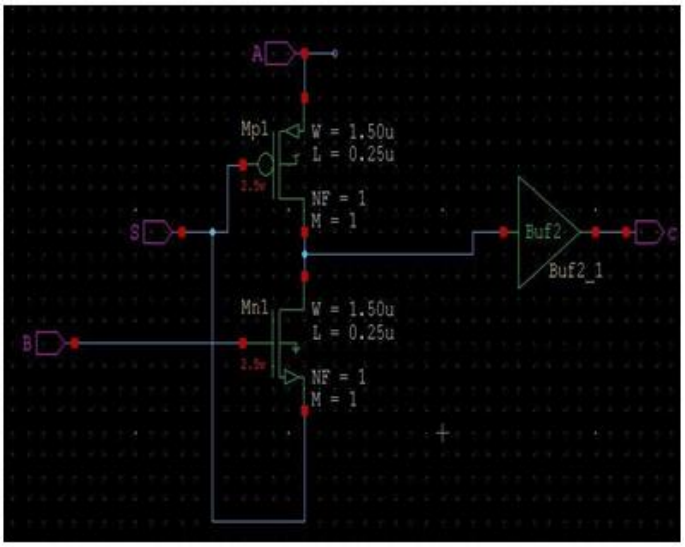

Fig 5:- MUX USING GDI

Selection Lines		Output
S0	S1	Y
0	0	D0
0	1	D1
1	0	D2
1	1	D3

Table 3:- MUX Truth Table

➢ *XOR gate implementation using GDI*

XOR logic gate gives a high output when the number of inputs is odd number of ones. The Boolean function for XOR gate cannot determined directly like AND, OR gates. As it is a Hybrid gate, the Boolean function of output of XOR gate is given by combining Multiplication, Addition and inverting of inputs.

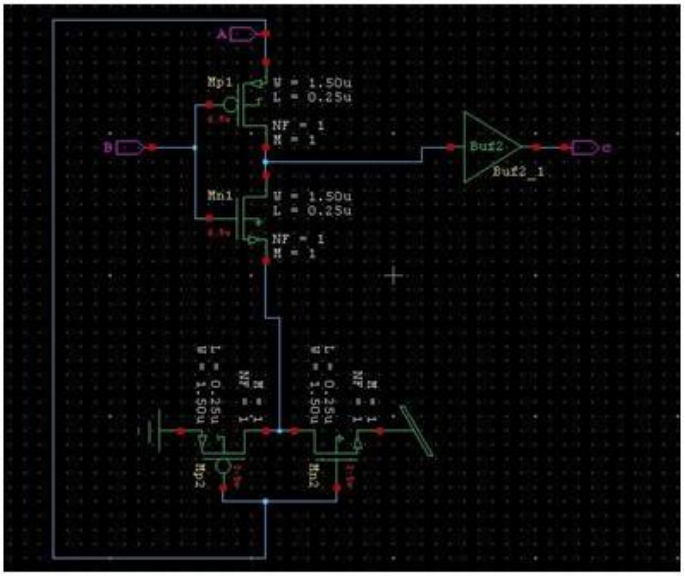

Fig 6: Schematic diagram of XOR using GDI

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In XOR based adder only one 2:1 MUX is used instead of two XOR gates. So, it requires only 6 MOSFETs. Whereas in conventional type adder, two AND gates and one OR gate is used. It needs atleast 18 number of MOSFETs.

Since it has minimum reduction of 12 MOSFET in XOR based 1-bit adders compared to conventional it contains low area and less consumption of power. Using optimistic values at the same time leads to a finer delay performance.

Elements of the circuit design, input, output values and delay of each transition, maximum working frequency, static and dynamic power dissipations of the new structure are discussed and calculated and the performance is compared with XOR gates which confirm that the presented structure has a high performance.

➢ *Implementation of Carry Select Adder (CSA) using GDI*

The carry select adder is a fast–parallel adder. It minimizes the propagation delay by more complex hardware. So, it is costlier. In the circuit making, the carry logic over fixed groups of bits of the adder is minimized to two level logic, which is nothing but a transformation of the ripple carry design. This technique makes use of logic gates so as to look at the lower order bits of the design and added to see whether a higher order carry is to be generated or not.

Input		Output
A	**B**	**Y**
0	0	0
0	1	1
1	0	1
1	1	0

Table 4:- XOR - Truth Table

A	B	Ci	Ci+1	Condition
0	0	0	0	Carry is not generated
0	0	1	0	
0	1	0	0	
0	1	1	1	Carry is not propagated
1	0	0	0	
1	0	1	1	
1	1	0	1	Carry is generated
1	1	1	1	

Table 5:- Carry Propagation conditions

Pi = Ai ⊕ Bi Gi = Ai Bi

The sum and carry outputs is given as

Si = Pi ⊕ Ci C i
+1 = Gi + Pi Ci

The carry-select scheme is to improve binary addition rate as shown in below figure. In this, two Ex-OR gates are required by each sum output. The first Ex-OR gate generates Pi variable output and the MUX generates C i +1 variable.

It is also realizable to construct 16 bit and 32-bit parallel adders by cascading the number of 4-bit adders with carry logic. A 16-bit carry select adder is constructed by cascading the four 4-bit adders with two more gate delays, whereas the 32-bit carry select adder is formed by cascading of two 16-bit adders.

The Carry Select Adder is established using a pair of XOR gates and a mux. Adding two numbers with CSA is nothing but addition of two numbers taking input carry first as 0 followed by second adder by taking input carry as 1.

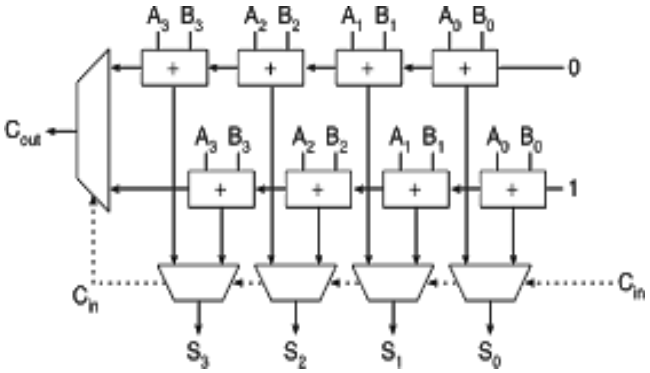

Fig 7: Block diagram 4-bit CSA

Relying on the inputs (carry-in, the sum and the carry-out of previous mux) of the multiplexer the output is obtained in the end. A 16-bit CSA has 16-full adders with the input signal as carry that transforms from one full adder stage to the next, i.e. from Least Significant Bit to Most Significant Bit.

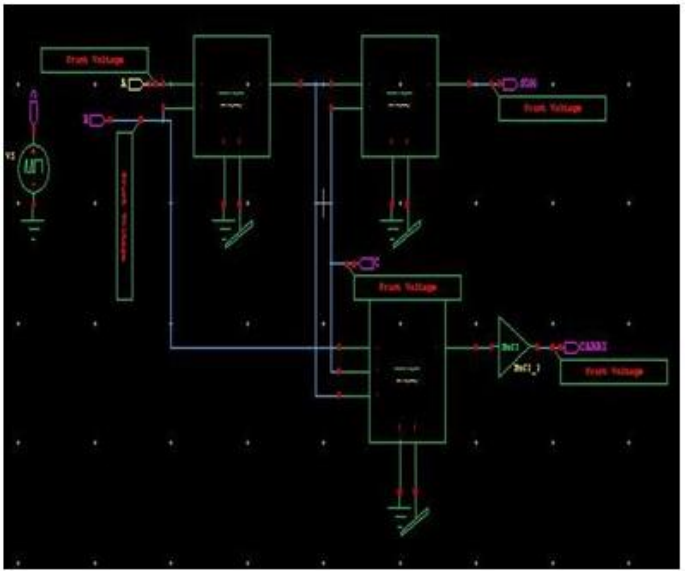

Fig 8:- Schematic diagram of 1-bit CSA using GDI

The schematic diagram and put-in and put-out waveforms of a 1-bit CSA are given in Figures 8 and 9 respectively. Since XOR based 1-bit adders have been used in the 16-bit CSA which are the main building blocks so the number of MOSFETs required is much less than conventional CSA.

Fig.9 Shows the Proposed 1-bit CSA waveform. It consists of three data input A, B and C. Depending upon the input given and based on the two XOR and MUX operation output will be carried out in the form of '0' or '1' through the SUM and CARRY in the waveform part.

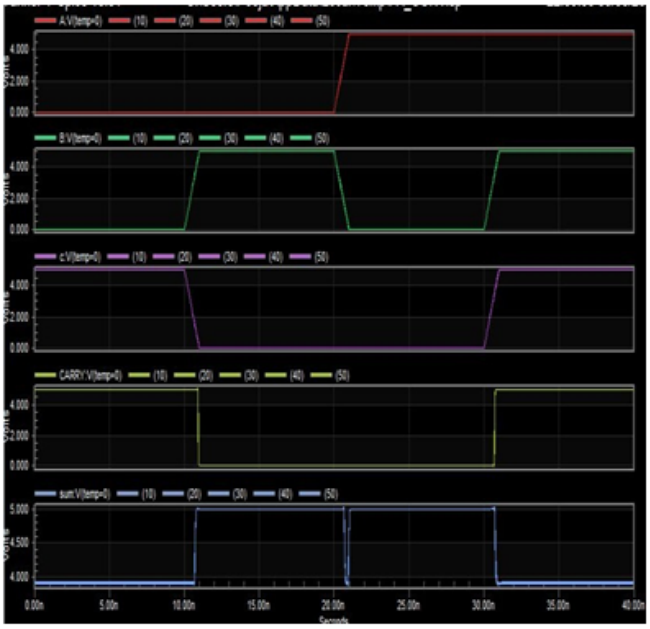

Fig 9:- 1-bit carry select adder - Input-output wave forms

Comparison Tables for Delay and Area between Conventional and GDI Based Full-Adder Cell Delay

Time between a 50% transition on input to 50% transition of output waveform. It is also called as Gate delay or Propagation delay. The gate/cell delay is not constant for all design environmental conditions. Cell delays are calculated using Non-Linear Delay Model (NLDM) and the cell/gate delay depends on the input transition and output load.

cell delay = {input transition time, Output load}

Logic Gates	Conventional Method	GDI Method
AND	1.45	1.09
OR	1.59	1.15
MUX	1.05	0.61
XOR	1.09	0.61
1-BIT FULL ADDER	3.10	1.45

Table 6:- Delay (s) difference between conventional and GDI based gates

➢ *Area*

Large chip areas need an absence of defects over that area. If chips are huge for a particular processing technology, there will be little or no yield. The unit λ, the fundamental resolution, which is the separation from which a geometric feature on any one layer of mask may be arranged from another. It need at least 1λ isolation from any other device or 25λ2 for the overall device area. Thus, a single transistor is 4λ2 , arranged in a minimum region of 25λ2 . Thus, the selection of the area unit is somewhat autocratic. Reducing the number of transistor usage reduces the area GDI Technique.

Logic Gates	Conventional Method	GDI Method
AND	6	2
OR	6	2
MUX	12	4
XOR	12	4
1-BIT FULL ADDER	28	10

Table 7:- Area (μm^2) difference between conventional and GDI based gates

➢ *Temperature effect*

The threshold voltage of a transistor depends on the temperature. A higher temperature will decrease the threshold voltage. A lower threshold voltage means a higher current and therefore a better delay execution. In GDI Technology delay measured as it remains constant with increasing temperature.

TEMPERATURE (degrees)	CONVENTIONAL 1-bit FULL ADDER (seconds)	GDI 1-bit FULLADDER (seconds)
0	2.15	1.29
10	2.14	0.74
20	2.20	0.75
30	2.23	0.75
40	2.25	0.75
50	2.26	0.75

Table 8:- Delay at different temperatures

Parameters	Conventional	Proposed (GDI)
No. of transistors used	28	10
Power (mW)	9.598	0.450
Area (μm^2)	752.343	442.485
Delay(s)	2.84	1.52

Table 9:- Comparison Table for 2:1 MUX

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V. SIMULATION RESULT

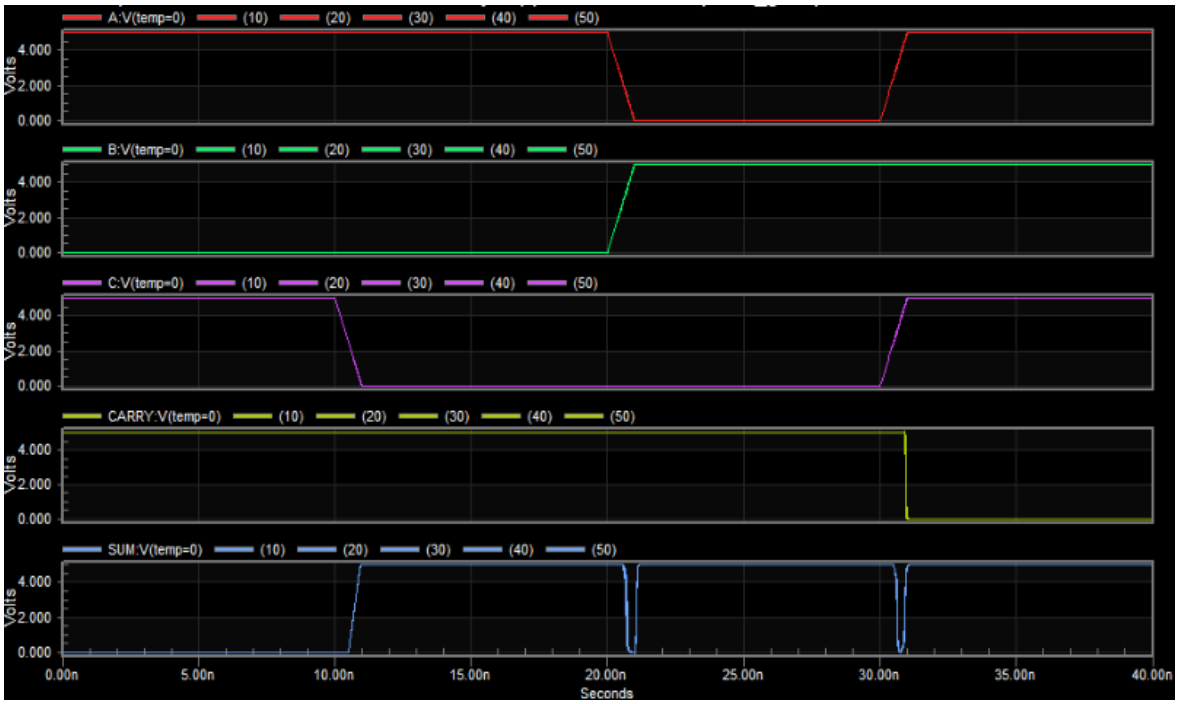

Fig 10:- 1-bit carry select adder - Input-output wave forms

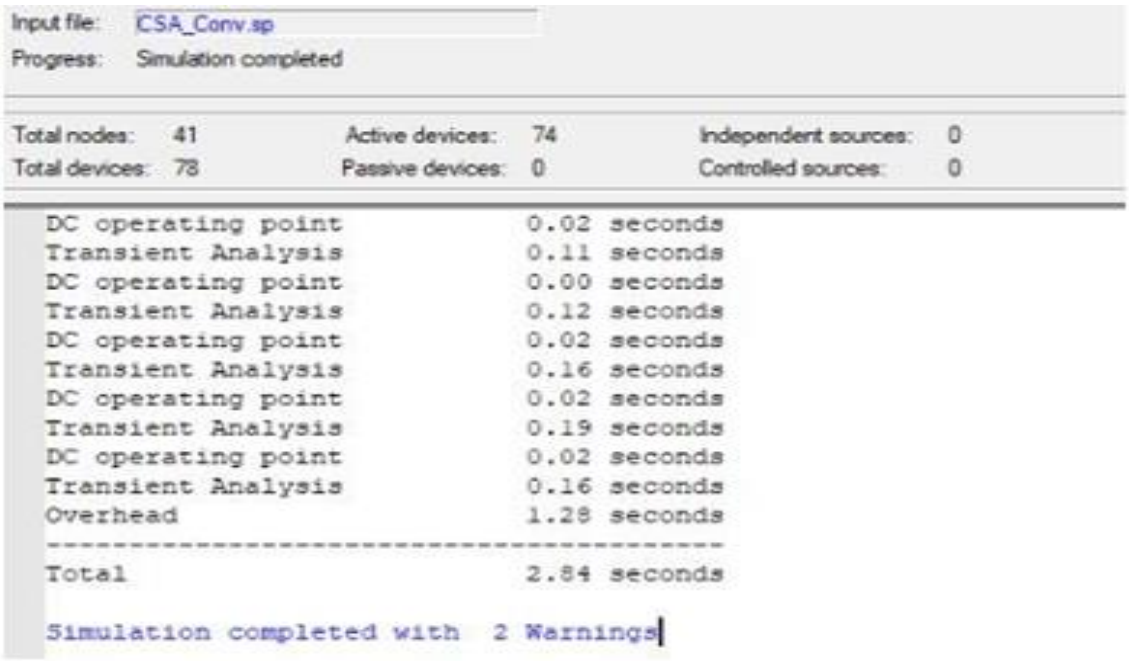

Fig 11:- Simulation result of Delay in Conventional based CSA

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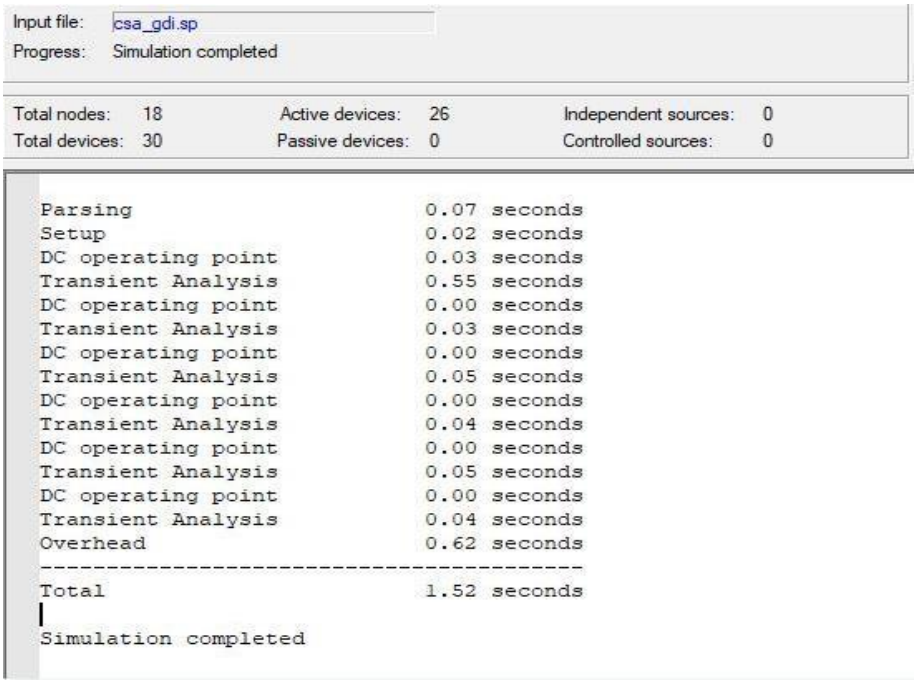

Fig 12:- Simulation result of Delay in GDI based CSA

VI. RESULTS AND DISCUSSION

The schematic diagram of Carry Select Adder is developed by utilizing Tanner tools and modified using GDI technology. The waveforms were observed using the WED tool in tanner software. The area occupied by the adder and delay generated is from TSP of Tanner tools. We get different values of delay at different temperatures. These are as shown in table below. From the above table, we can say that the increase in temperature leads to decrease in delay in GDI technology and also it is much less than the conventional method. In this, we compared only for 1-bit carry select adder which can be applicable to n- bit also.

VII. CONCLUSION

1-bit carry select adder is constructed using 1bit full adder based on GDI technology as a basic building tool. In this, larger area and delay get reduced. In this, Area reduced by 79.16% and delay from 2.84 to 1.52 seconds i.e 46.47% delay gets reduced. Thus, if is applied to n-bit adders' larger amount of area and delay gets reduced.

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