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An Efficient Viterbi Decoder for Low Complexity, High Performance Digital Systems

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Abstract:- The level of circuit performance which can be reached with in certain design time mainly depends on the efficiency of the design methodologies as well as on the design style. In digital design researchers interesting in decrease the consumed power, area as result the speed of the system increases. By using reversible logic which has advantages over traditional one such as decrease gate counts and garbage output in addition to constant inputs. In this paper design of Viterbi decoder based reversible gates is presented and verified using Xilinx.

Keywords:- *Reversible Gates, Viterbi Decoder, Simulations and Results .*

I. INTRODUCTION

The Viterbi translating calculation was presented by Andrew J Viterbi, which is a decoding process for convolutional codes in memory-less clamor. This calculation is actualized in the structuring of correspondence frameworks. The Viterbi Algorithm is the most asset expending and it finds the probably quiet case progress grouping in a state graph, given an arrangement of images which are hindered by clamor [2]. For the most part, a Viterbi decoder consists of three main calculation units: fig 1

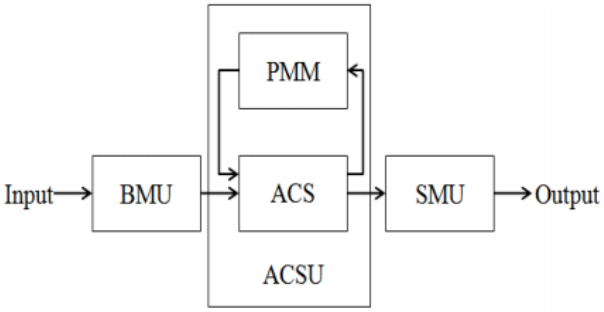

Fig 1:- Main parts of Viterbi decoder

Main part is known as branch metric unit (BMU), which contrasts the got information images and the perfect yields of the encoder lastly the branch metric will be determined. The Euclidean separation or Hamming separation which is applied for the computation of BMU. The BMU creates branch measurements for the accompanying module regarding the images obtained by the channel.

The Add Compare Select Unit (ACSU) is described as all Branch Metrics (BM) to the following Path Metrics (PM). The new PM will be thought about and the chose PM will be put away in the Path Metric Memory (PMM). Simultaneously, the ACSU stores the related survivor way choices in the Survivor Memory Unit (SMU).The PM of the survivor way of every state is refreshed and put away inside the PMM. The rest of the Memory Unit utilizes the Trace-Back technique to recognize the survivor way and yield information. The decoded bits which are included in this unit will be eliminated from the beginning through minimal way metric.

Initially start with second state, in reverse following is 5 went after by the 6 survivor way, initially first added to the 8 and a 9 one way is distinguished. While tracking2 back 3through the trellis, the decoded 5output succession corresponding7 to the traced8 branches9 is generated0 in the switch request.

II. REVERSIBLE LOGIC

Reversible registering is the utilization of standards of reusing to figuring. A reversible rationale door is mapped with coordinated rationale gadget having a n-input, n-yield entryway. As it discovers the yields from sources of info despite the fact that the information sources can be only recouped from the yields. In the vital conditions to have the quantity of sources of info equivalent to the quantity of yields extra data sources or yields is included. A significant requirement presents on the structure of a reversible rationale circuit utilizing reversible rationale door is that the fan-out isn't permitted. The quantum cost of reversible rationale circuits must be least. With the base number of reversible doors, the structure of reversible circuit is cultivated.

The real limitation to accomplish enhancement of the circuit is to deliver the trash yields and the consistent contributions with the base number. The reversible rationale entryways are the circuits which has number of sources of info is equivalent to number of yields.

The significant improvement parameter for each reversible rationale entryway is the quantum price [4]. The necessary elements for Viterbi decoder are listed below:

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➢ *Feynman Gate*

The Feynman door is 2x2 reversible entryway which include the information sources (A, B) and produce (P =A, Q = A B). This door is likewise alluded same Controlled NOT. The quantum price is 1. This is chiefly utilized for the fan-out capacity. The used power and deferral are 17mW and 7.761ns [3].

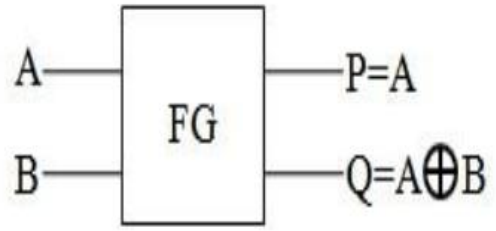

Fig 2:- Feynman Gate

➢ *Peres Gate*

The Peres door is 3x3 reversible entryway, in which the A, B,C are the sources and P, Q and R are represented outputs . The outputs are mapped as P =A, Q = A B and R= A.B C. The quantum price is 4,and the used power and time are 24mW ,7.824nsrespectivily.

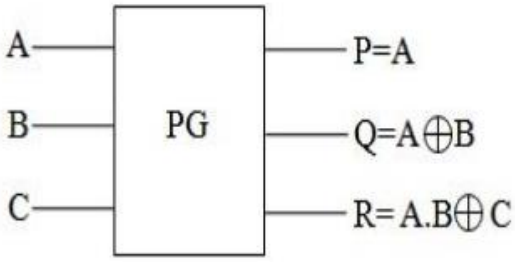

Fig 3:- Peres Gate

➢ *HN Gate*

The HNG is a 4x4 reversible gate with four inputs A, B, C, D and four outputs P, Q, R, S, where P=A, Q= B, R= A B C and S= (A B) C AB D. The quantum price is 6 and the consumed power with delay are 24mW and 7.823ns.

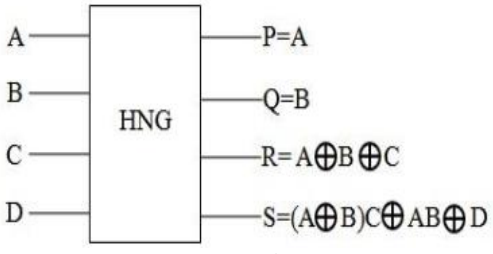

Fig 4:- HN Gate

III. SIMULATION AND RESULTS

The proposed Viterbi decoder is simulated by Verilog coding and recreated. And simulation results are shown in figs (5-17) The most important parameters for evaluate VLSI configuration are area, power and speed. Table 1 summarize The execution power report and Table2summarize area and timing report.

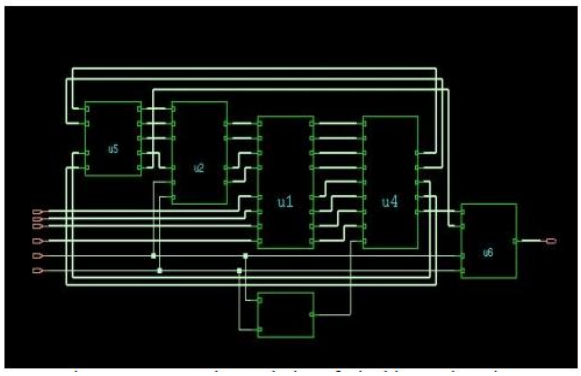

Fig 5:- RTL design with reversible logics

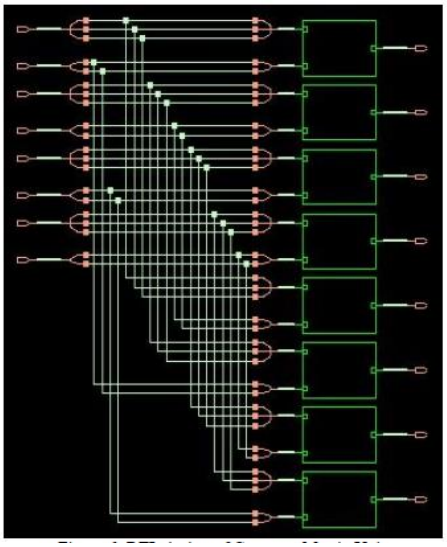

Fig 6:- Compute Metric Unit RTL design

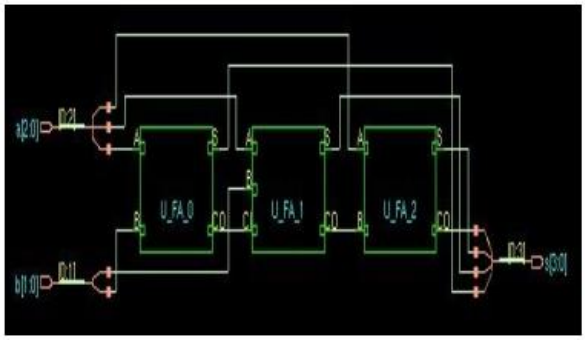

Fig 7:- Compute block of RTL design

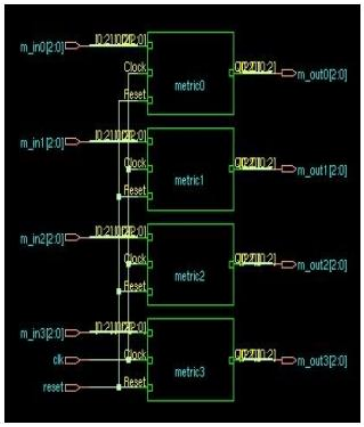

Fig 8:- Metric Unit design (RTL)

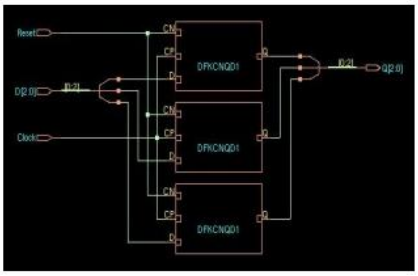

Fig 9:- Design of Metric unit with D flip flop

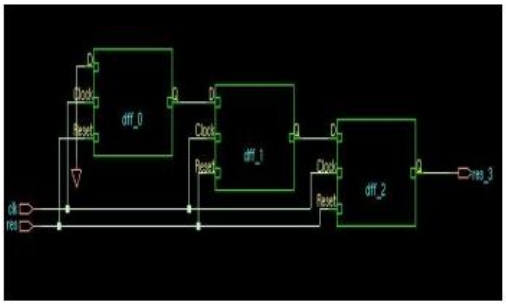

Fig 10:- ACS-Enable Unit design(RTL)

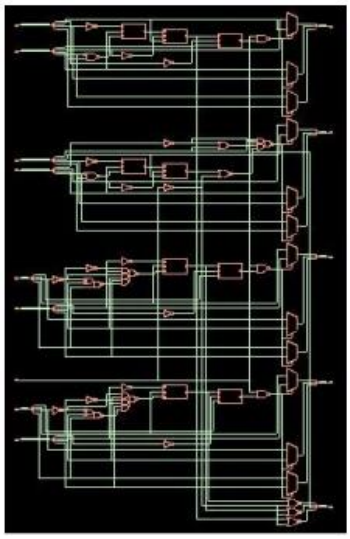

Fig 11:- Compare Select Unit design(RTL)

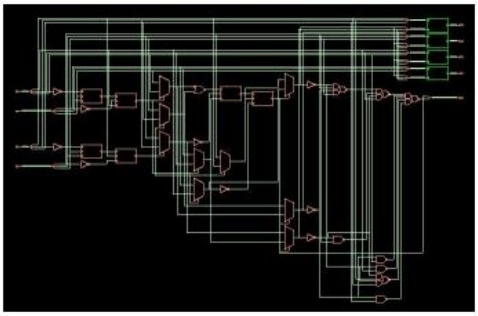

Fig 12:- Reduced Unit design (RTL)

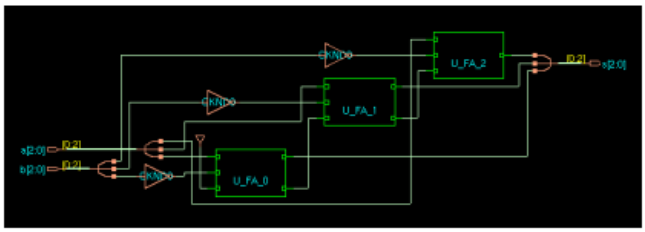

Fig 13:- Reduced Unit design with two inputs

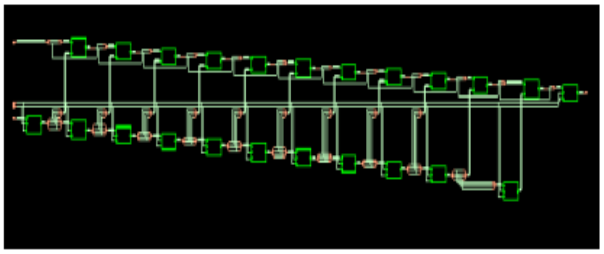

Fig 14:- path memory unit design(RTL)

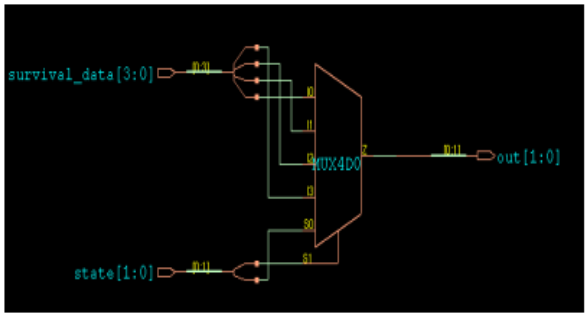

Fig 15:- multiplexer units 4x1)

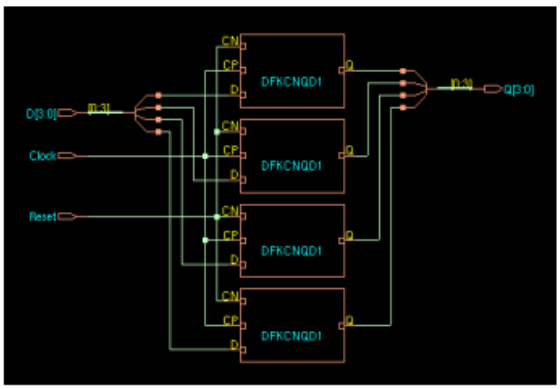

Fig 16:- Buffer unit with D-flip flop

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IV. RESULTS AND DISCUSSION

INSTANCE	Power Analysis in ηW		
	Leakage Power	Dynamic Power	Total Power
U1 [Compute Metric]	1436.774	4871.918	6308.693
U2[Metric]	555.193	2961.352	3516.545
U3[ACS_Enable]	157.896	298.383	456.279
U4[Compute Select]	520.295	3986.532	4506.828
U5[Reduce]	1000.059	5939.455	6939.514
U6[Path Memory]	2697.978	11326.026	14024.004
VITERBI [TOP LEVEL]	**6368.196**	**30094.526**	**36462.722**

Table 1:- Power Performance Summary

INSTANCE	Number of Cells	Area (sq microns)	Time Delay (psec)
U1 [Compute Metric]	40	173	320
U2[Metric]	12	86	135
U3[ACS_Enable]	3	22	0
U4[Compute Select]	51	111	533
U5[Reduce]	74	177	1343
U6[Path Memory]	57	422	2213
VITERBI [TOP LEVEL]	**237**	**990**	**4544**

Table 2:- Summary Performance of Area and Timing

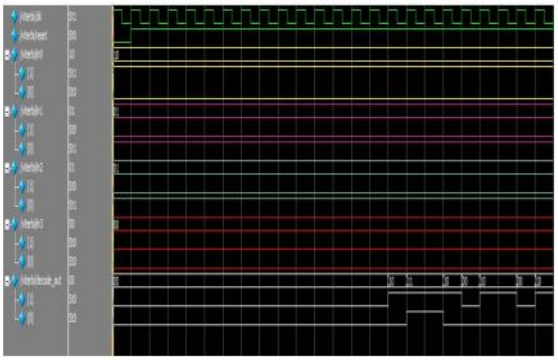
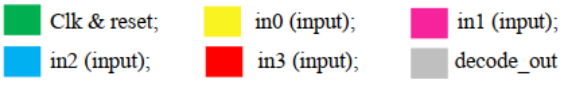


Fig 17:- Output waveforms



V. CONCLUSION

In this paper vertibi decoder is designed using reversible logic gates which have advantages over classic gates such as reduction in consumed power and reducing area. The designed decoder is verified by Xilinx and the results showed that it has less power consumption and less area so it may be used in high performance digital systems.

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