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Investigating Buck Converter with Hybrid LDO Mode for Improved Low-Load Operation

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Abstract**:- Traditionally DC-DC step down converters or Buck converters exhibit better efficiency over a dynamic range of load conditions, comparing to linear regulators. This makes it suitable for wide array of applications. But coming to low load conditions, the losses rises, and overall efficiency reduces. Which makes this non-ideal for low power application and portable designs. This paper investigates the improvement of the low load operation with a new proposed system, comparing to existing methods. The proposed system, targets to transfer the converter to LDO operation when low-load conditions is detected. The inherent advantages like low ripple voltage, zero acoustic noise, improved efficiency is projected with this modification.**

Keywords*:- Buck Converter, LDO, Efficiency, Ripple Voltage, Acoustic Noise.*

I. INTRODUCTION

DC to DC conversion is pretty much inevitable unit in every electronics designs. Conversion is probably an input DC voltage to another DC voltage, to source one or more loads within the circuit. This can be increasing the voltage from one level to another (step up), decreasing voltage (step down) or increase/decrease based on system condition (step up/down). The ideal behaviour is that the sum of power provided to the input ports must be the same from the output ports of the converter block. This can be said in another words as converter with 100% efficiency. But practically, several losses introduced into the system and the efficiency will be permanently less than 100%. Still the design objective of DC-DC converters to make the efficiency close to maximum. In the bird eye view, there is two type of regulators, linear and switching regulators. Both are highly useful based on the design instances they are selected.

Basic difference is that Linear regulators involve an ohmic element to reduce the voltage from input to output ports by dissipating energy. This is useful for low output current situations. Also, the control circuit of linear regulators are faster, the Power Supply Rejection Ratio (PSRR) and output ripple voltage can be better, makes it sutiable for some of the analog and RF circuits. Switching regulators involve switching elements to turn ON and OFF at desired instances and along with L-C circuit, implements voltage conversion. Here step up, step down & step up/down are possible. Whereas with linear regulators its always and only step-down conversion. Also, the efficiency is better for higher and mid current levels, makes it appropriate for wide range of application.

In this paper specifically interested in step-down converter or Buck converters. Generally buck converters yield approximately >85% of efficiency at mid to high output conditions, for a given switching frequency. But when the load conditions drop, say below 20% of maximum load, efficiency plummets. In this condition buck converter will be working in Discontinuous Conduction Mode (DCM). For an application which require a wide spectrum of load currents at given volage, this property of buck will be a hiccup.

As mentioned earlier use of linear regulator (or specially LDO) at low-load condition is more acceptable comparing to buck converter. This is because the efficiency of LDO is a function of output current. With less current, it is more efficient. But majority of the modern applications need voltage regulators to be operatable for a wide range of output current. Thus, LDO is suitable for only a specific region in the operating spectrum. Thus, merely using the LDO or buck converter is not the best solution.

II. EXISTING SOLUTION

Buck regulators is constituting of switching section and LC low pass filtering section. The switching section extends the possibility of changing the way it operates. Nowadays, based on system requirements such as load, noise, regulation and Q-factor, the mode of switching is selected or dynamically varied.

A. *PWM Based Converters*

Conventional method of switching is using pulse width modulation (PWM). The switch in the buck regulator is a transistor, and generally a MOSFET. The PWM signal will be given to the gate of the MOSFET, results in the desired switching cycle. The PWM will be characterised by a fixed frequency and variable duty cycle. The duty cycle is responsible to define the output voltage level of the regulator. Based on the PWM the input DC voltage is truncated and passed through the LC circuit, to profile into the average value, which is required output voltage. This is the basic and simple operation of the buck converter. A flyback diode is present in the circuit to avoid voltage spiking across inductor. This diode will be replaced with another switching transistor in synchronous buck converters.

The practical circuit of PWM based buck converter is comes with multiple loss components. Majorly switching losses and conduction losses makes the efficiency of the regulator lower than the ideal conditions. Conduction losses arises due to the different ohmic losses. Specifically, at MOSFET (RDS on), copper loss at inductor, loss at flyback

diode, and at Capacitor ESR are some examples. These losses increase with operating current. Use of synchronous converter is an approach to mitigate the loss at flyback diode. But still majority of other loss components are difficult to eliminate. Switching losses are occurring due to the different switching nodes. MOSFET is one of the major components here. When transistor shift through ON to OFF states, for an instant it resides in the saturation region and offers a DC resistance to the current flow. The flyback diode has the inherent reverse recovery property causes unexpected flow of current for a short duration when diode made reverse biased. This behaviour also causes loss. The magnetic characteristics of the inductor also contributes to efficiency reduction. Likewise, there are other components also introduces the loss such as the gate driving circuit and capacitors. In nutshell switching losses are majorly depended on switching frequency.

The typical efficiency of the PWM based converter is above 85% for normal conditions. The power circuit and its control loop are designed in a way to get the maximum efficiency and regulation. But when the load current decreases with fixed switching frequency, the switching losses elevates. Even though, the conduction loss is reducing, the increment in the switching loss in more dominant. This results in drastic reduction in the overall converter efficiency. When perceiving the efficiency characteristics of the converter, values maintains high at certain load conditions and at low load its falls.

B. *PFM Based Converters*

Pulse Frequency Modulation (PFM) based converters are now offered in the market. These are modified from PWM based operation. The major change can be observed here is that low load efficiency is improved comparing to traditional buck converter.

Primary change is happening on the gate driving circuitry. Instead of switching the MOSFET with fixed frequency and at adjustable duty cycle, in PFM mode the switching translates to variable frequency with pulses of fixed width. This is more over a Current-based regulator operation as opposes to the Voltage-based in PWM mode.

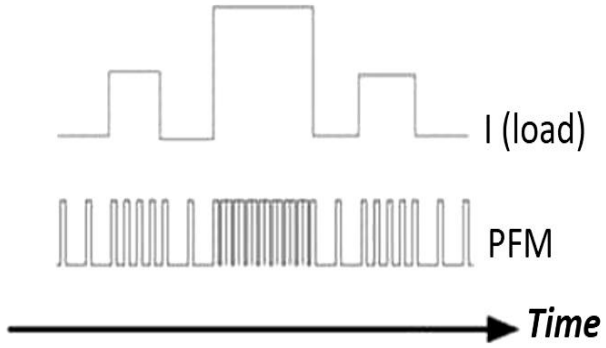

Fig. 1 Illustration of PFM with Load Current

When the load current requirement increases a more number of pulses will be generated and load will be provided with more current. Same way when the load current reduces, the frequency of the pulses decreases. The decision of selecting the frequency is done at the gate driving section with the feedback from the control loop.

Generally, these types of regulators will not be available as standalone solution. This implemented as an integral mode with PWM mode. As discussed, PWM solution is favourable for mid and high current scenarios and whereas PFM solution preferred for the low current operation. PFM mode has certain limitations when try to operate at the higher current levels. As the number of pulses needs to increase, beyond a point the pulse count saturation will occur, and no further increment will be possible.

Accordingly, both modes are incorporated into single controller chip. And based on the load condition, mode of operation will be designated as either PWM or PFM. Inductor current in the power circuit is needed to monitor continuously to switch between modes. When the inductor current is lowering than the threshold, then regulator switches to PFM mode. Similarly, when current goes up again, automatically operation switches back to PWM mode.

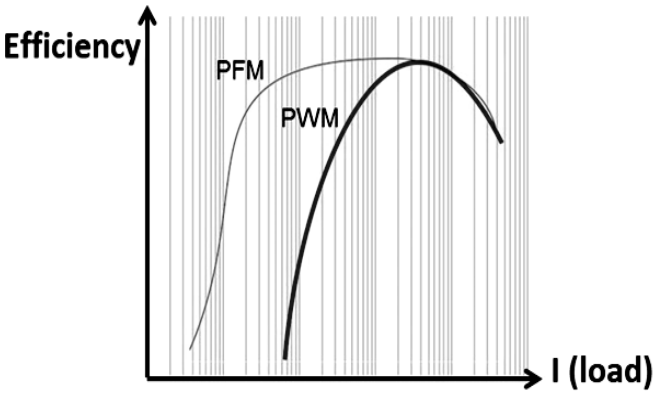

Fig. 2 Efficiency Comparison: PWM & PFM

As the switching frequency dynamically lowers at the low output conditions, majority of the switching loss can be minimized. This results in an improved efficiency characteristic comparing to the PWM mode. Refer the figure 2 for the comparison.

III. PROPOSED METHOD

The intention here is to improve the performance of buck converter specifically at low load conditions, provided other load conditions are not affected. As observed from the past designs, PWM based solution is not performing well for low load conditions.

The proposal is to implement an LDO mode at lower output current situations, preserving conventional mode of operation at higher levels. When the load current is falling below the threshold level, the buck converter operations switches to LDO operation. Refer fig 3 for understanding the change in operation. Primarily by changing the primary transistor from switching to amplifier. With the amplifier operation the transistor acts like a variable resistor in the power path, which controlled by the gate circuitry. Like an LDO, here the input voltage is step down to a new value by

dropping the delta value over the transistor. Remaining part of the power circuit will remain physically same. Such as the flyback diode, inductor, and the output capacitors. The inductor and capacitors form a second order low pass filter, which further aids the removal of noise from the generated voltage. (Whereas in the buck converter, these components were involved in the current ripple limiting, AC filtering, wave shaping). The flyback diode will remain in shut down, and not involved in the operation. The implementation is not requiring any changes in the board level. Modification will be done in controller chip design. Which makes the platform design remains same, while one time change in the die is only required.

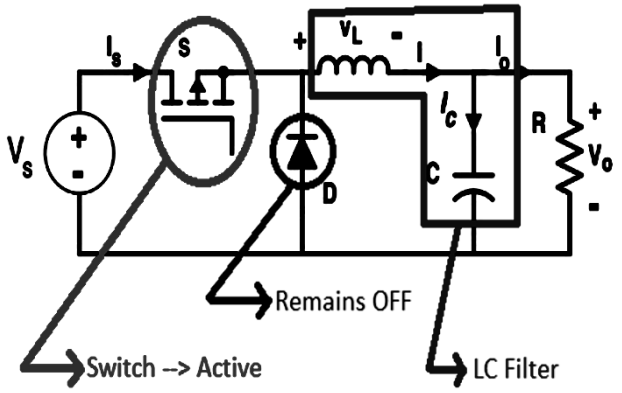

Fig. 3 Change in operation at power circuit

The design of the gate driving circuit is the critical change required to implement this design. As the proposed solution interested in the multi-operation, the gate driving circuit must be modified to more be versatile. In case of PWM or PFM the region of operation is in the switching. But when LDO operation is required, transistor should work in the saturation region (assuming MOSFET is used). The biasing of MOSFET must change based on the inductor current feedback. The same current feedback mechanism used in the current PFM based buck converters can be adopted here as well.

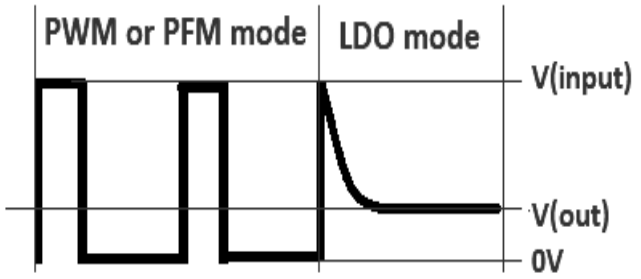

Fig. 4 Transition from switching mode to LDO mode

The proposed system can be used in synchronous and asynchronous mode operation in the buck converters, as the flyback diode or lower transistor is not involved in the operation. In the context of the multiphase operation further studies is required. Scope of this paper is restricted to single phase conversion. The LDO operation is proposed to implement two ways in the application level. The two approaches are explaining in below sections.

A. *PWM-LDO Approach*

In this approach, buck converter shall operate in PWM mode under normal operations. When the trigger event occurs, transistor will be biased to LDO operation, and maintains the output voltage. This is the simple approach and recommended for very low power operations. The transition of operation is illustrated in fig 4.

B. *PWM-PFM-LDO Approach*

When dealing with relatively more power, this approach is more suitable. Like existing PWM-PFM converters, this converter works in the PWM and the PFM modes in high and mid load conditions. When the trigger occurs at low load, then it switches to the LDO mode. Consequently, there is three levels of operations, which makes it complex in design but more power efficient.

IV. ANALYSIS

The major advantage of use of LDO mode under low current operation is the reduction in losses. Also, the generally the response of transistor in saturation is quicker, thus the regulation becomes easier. This outcomes in a reduced output ripple voltage. The absence of the switching improves the system's EMC performance at this conditions. LDO operation also required comparatively low output capacitance, makes the output capacitance designed for the PWM/PFM operation sufficient.

PFM is a promising technology in terms of improving the regulator performance. On comparing with PWM method, PFM has miniscule power loss. It offers a smooth transition when the operation is changing from PWM. Few down sides of PFM methods are involving acoustic noise and output ripple voltage. As based on lower load requirement, the pulse frequency goes low around 20kHz or less, makes it audible. This usually creates inconvenience in the user environment. By selecting proper output capacitor, acoustic noise can be reduced in some extend. The frequency reduces means few voltage pulses are going to the output capacitor makes the ripple larger.

LDO mode doesn't produce any acoustic noise. Efficiency improvement is only applicable for selected window input and output voltages. As their voltage difference increases, efficiency declines.

V. CONCLUSION

Incorporating the LDO operation into the standard buck converter provides its own advantages. Major parameters like efficiency, acoustic noise, output voltage ripple, regulation, PSRR are improved in low-load condition. When comparing with PFM mode efficiency improvement is getting limited. Other parameter improvements are also preferred only based on the system requirements. Reaching a binary decision to adopt hybrid mode in the buck converter operation is difficult. But can be selected on the specific use cases.

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