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Reduction Techniques for Power and Delay on Full Adder by XOR Gate Logics Using Microwind EDA Tool

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Abstract:- Full adder circuit is central to most digital circuits that slaves a significant port in the design of particular integrated circuits. Power dissipation and delay are the momentous parameter of the circuits. Therefore reducing power consumption and delay in full adder and XOR gate using various logics like, Transmission gate logic(TGL),Pass Transistor logic(PTL) and static complementary metal oxide semiconductor (CMOS)logic, Dual rail Domino Logic and Domino Logic , Double Pass Transistor (DPL).The circuits are designed and implemented, simulated using Microwind EDA tool. Using the comparative power and delay analysis, the designer requiredan sufficient adder design can be select based on the parametercriteria.

Keywords :- *Transmission gate logic, Pass, Transistor Logic , Double Pass Transistor Logic DPL, Domino Logic, Dual rail domino logic , Microwind EDA.*

I. INTRODUCTION

Addition is the term used to describe adding two or more numbers together. Adder is basic building block of most digital system. All field of engineering have role of adder to produce arithmetic operation.

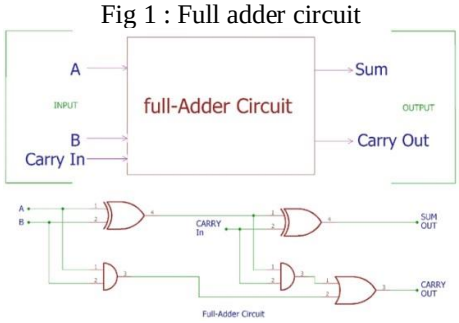
A. Adder :

An adder is acircuit that performs addition of numbers . Its process is to calculate address , table indices and similar operation.

B. Full adder :

Full adder is an arithmetic circuit that is used in many IC design. The block diagram of full adder is shown above. It has 3 input and 2 out put.

Fig 1 : Full adder circuit



➢ *XOR gate*

XOR represents the inequality function. It is a special type of logic the output true if the inputs are different. The inputs are same the output is false.XOR gate is made by the combination of three basic gates (AND gate , OR gate, NOT gate)

The power consumption will be decreased in full adder by designing the XOR gate in properways. XOR implements the application oriented digital circuits design.

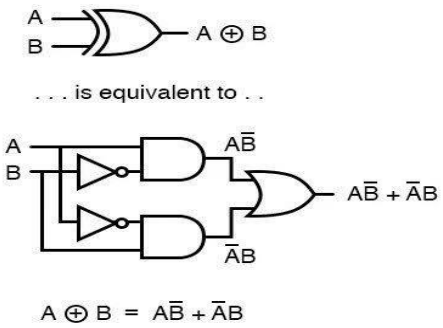


Fig 2 : XOR Gate

C. Power dissipation

The power dissipation play a major role to design any circuit.

With respect to power there are two major categories . They are,

1. Static Power Dissipation
2. Dynamic Power Dissipation
3. Short circuit power dissipation

D. Static Power Dissipation

Static power is the power it can be seen that one of the transistor is always off when the gate is in either of logic states. and is generally determined by the formula. Pstatic=Istatic.Vdd

E. Dynamic power dissipation

Dynamic power dissipation is the modeled by assuming that the rise and fall time of the step input is much more then the repetition period. Pdynamic=Pcap+Ptransient =(CL+C)(Vdd)^2fN^3

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F. short circuit power dissipation

It depends upon charge of capacitor. As the load capacitance is increased the significance of the power reducedby the capacitive dissipation Pd

Pshort=Ishort.Vdd

G. Delay

The delay is defined as the average of the low to High time and high to low time and is generally determined by

Tp=t(PLH)+t(PHL) / 2

II. PROPOSED METHOD

In this project ,we are going to design low power full adder by using XOR gate with various techniques. The six power and delay reduction techniques are,

1. Complementary metal oxide semiconductor (CMOS) logic
2. Transmission gate logic (TGL)
3. Pass Transistor Logic (PTL)
4. Domino Logic
5. Dual Rail Domino Logic
6. Double Pass Transistor Logic (DPL)

1. CMOS Logic

CMOS can be obtained by integrating the NMOS and PMOS device on the same substrate. It is immune toward noise occurring condition. It is also used in designing integrated circuits, microprocessor and microcontroller. The CMOS provide robustness against voltage scaling. It operatedhigh reliability and provide required power with minimum number of transistors.

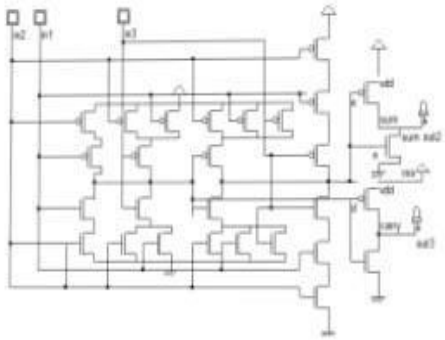

Fig 3 : CMOS Full adder

2. Transmission gate logic (TGL)

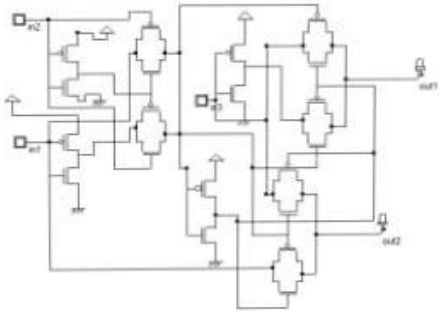

Fig 4:TGL Full adder

A Transmission gate is similar to a relay that can conduct in both directions or block by a control signal with almost any voltage potential. The Transmission Gate Logic full adder is called as Zhuang full adder. transmission gate is the CMOS based switch in which PMOS passes a strong 1 but poor 0 and NMOS passes strong 0 but poor 1.When the control voltage is high ,the gate is turned on with both transistors able to conduct. TGL providing a most voltage level at the output. because it consumes nearly half the ability consumed by a standard full adder.

3. Pass Transistor logic (PTL)

Pass electronic transistor logic (PTL) describes many logic families employed in the look of integrated circuits. It reduces the count of transistors used to make a completely different logic gates, by eliminating not use transistors.

Transistors are used as switches to pass logic levels between nodes of a circuit, rather than as switches connected on to offer voltages. This reduces the quantity of active devices

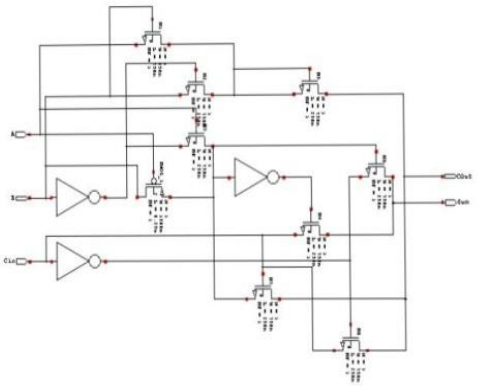

Fig 5: PTL Full adder

4. Domino logic

Domino logic could be a CMOS-based evolution of the dynamic logic technique.It purely depends on clock signal.The clock signal only decide a transistor as a precharged and evaluation switch. It had been developed to hurry up circuits, finding the premature cascade downside, generally by inserting tiny and quick pFETs between domino stages to constrain the interstage cascade rate to a curtailed a not require clock interlocks.

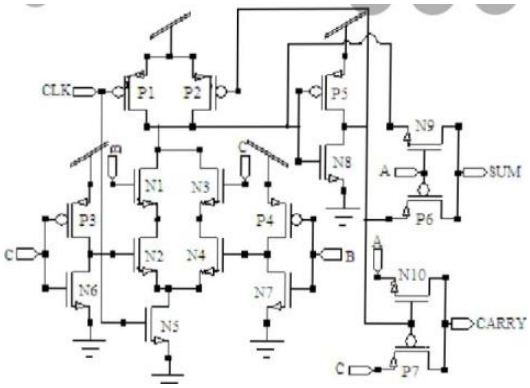

Fig 6: Domino Logic Full adder

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5. Dual rail domino logic

Dual rail domino provides both inverting and non inverting functions, added tothat is the clocking power. Firstly, if the clock for stage i+1 arrives earlier than the clock for stage I , stage i+1 is in evaluation where as stage I is still in pre-charge. The "precharged" output of stage I when fed to the gate terminal of the NMOS transistors used in stage i+1 turns the aforementioned NMOS transistors ON and thus the output of the NMOS Block discharges and remains permanently at logic low, thus preventing the NMOS block from simulating the required functionality.

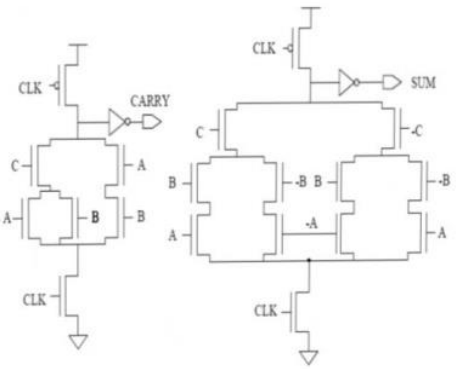

Fig 7 : DRDL Full adder

6. Double Pass Transistor logic

DPL represents a PTL family alternative to CPL.This eliminates problem of the threshold drop and use of inverting after each block. DPL is shown to boost circuit performance at reduced offer voltage. Its symmetrical arrangement and double transmission characteristics improve the gate speed while not increasing the input capacitance .we propose a differential logic unit enforced in CMOS double pass junction transistor logic. The planned logic unit (LU) is low power and tiny variety of transistors style. It performs eight logic functions with solely sixteen transistor.

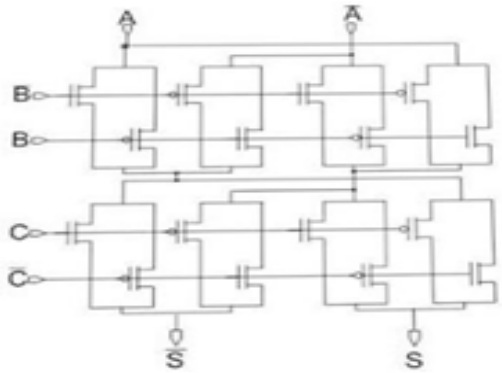

Fig 8 : DPL Full adder

III. RESULTS AND DISCUSSION

The circuit of the six different power and delay reduction techniques of full adder with XOR gate designed by using MICROWIND tool and its layout be generated with the help Microwind EDA editor and its functionalities are verified in each style.

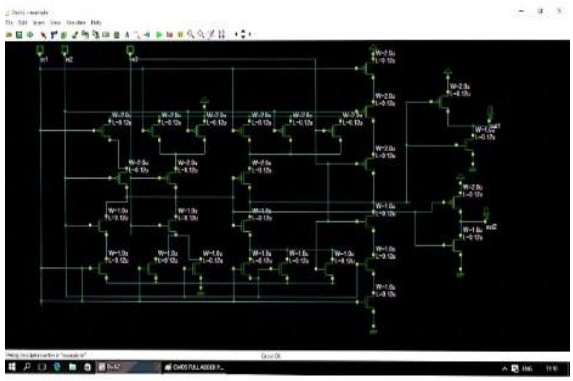

Fig 9:CMOS full adder circuit

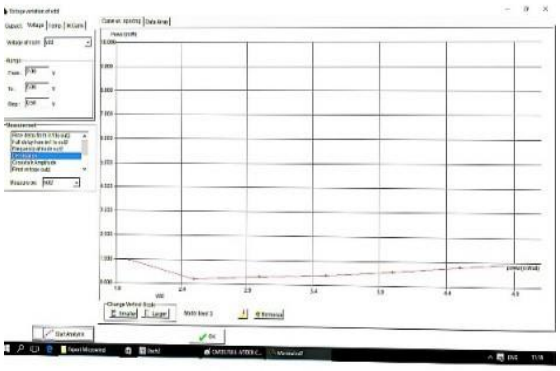

Fig 10 :power dissipation of CMOS

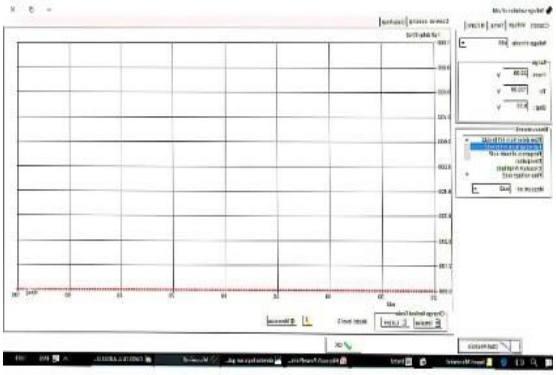

Fig 11 : Delay of CMOS full adder

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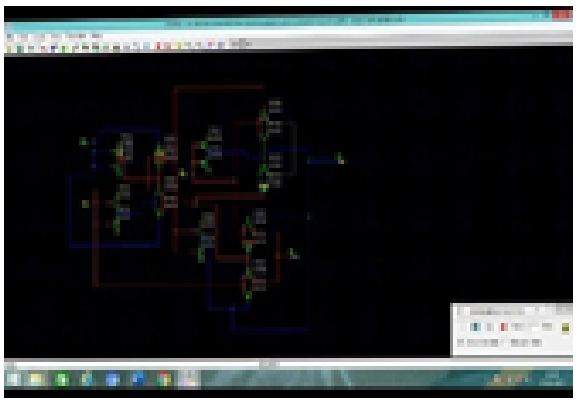

Fig12:TGL Full adder Circuit.

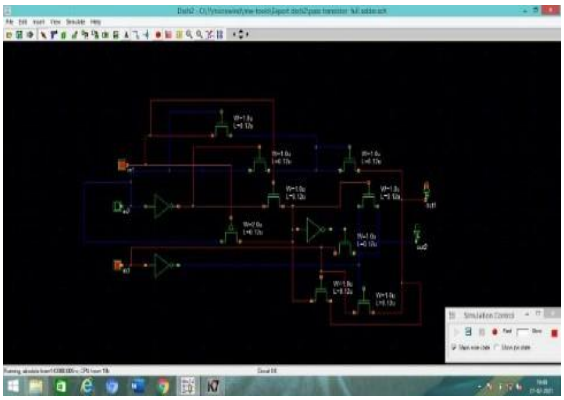

Fig 13 : power of TGL Full adder.

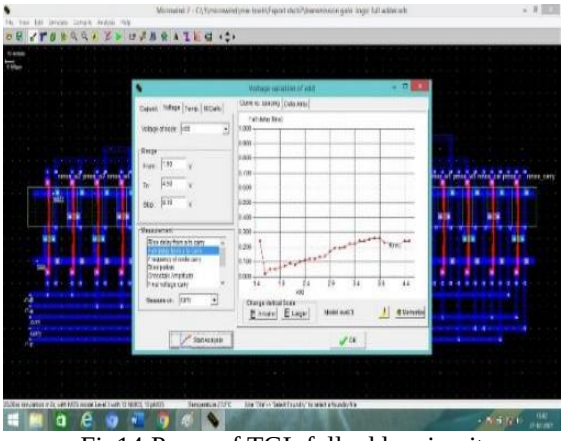

Fig14:Powerof TGL full adder circuit

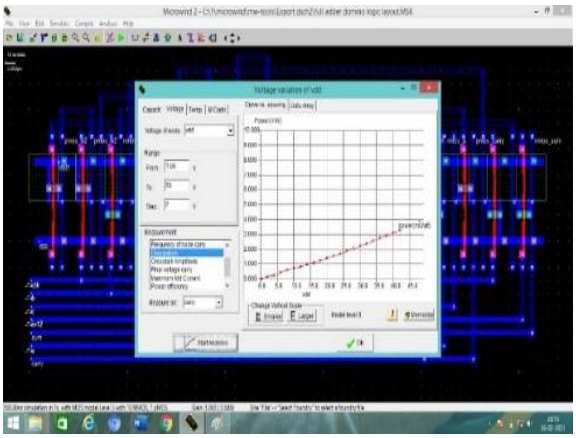

Fig 15 : delay of TGL output

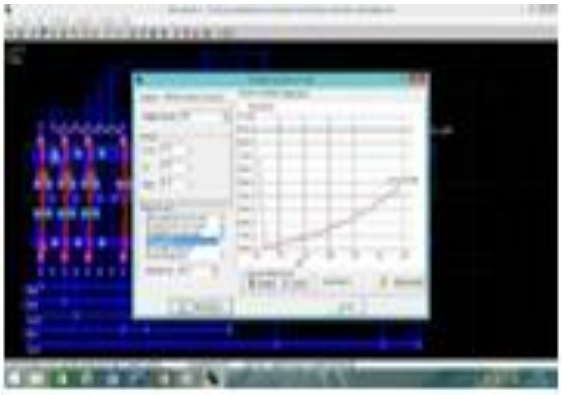

Fig 16: power of PTL full adder

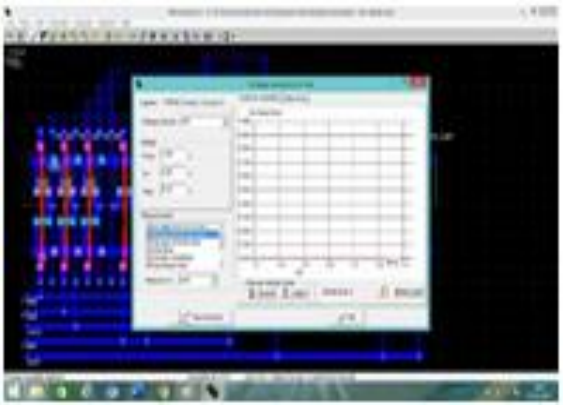

Fig 17: delay of PTL full adder

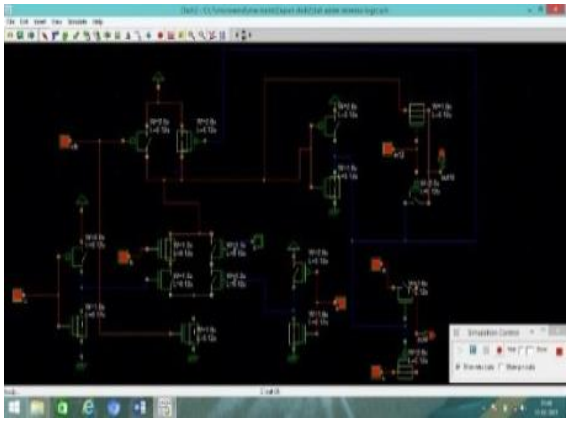

Fig 18: Domino Logic full adder

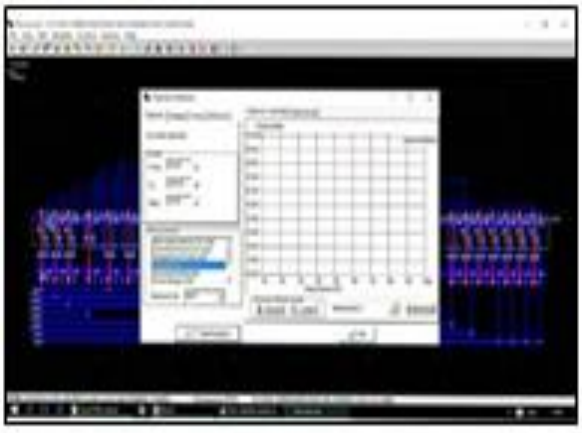

Fig 19: Domino Logic power

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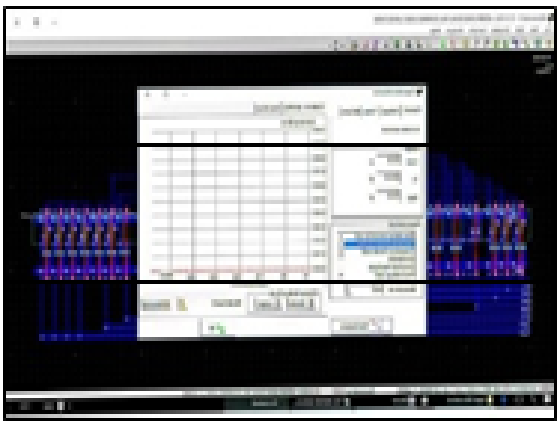

Fig 20 : Domino Logic delay

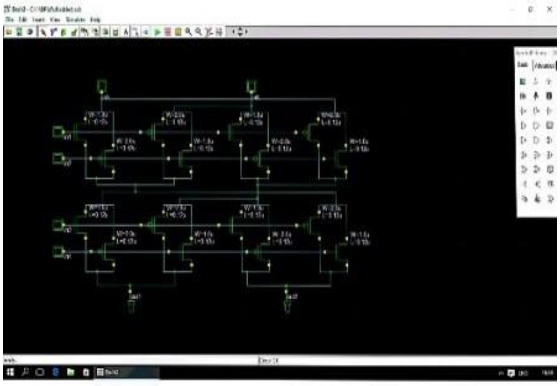

Fig21 : DRDL Full adder Circuit

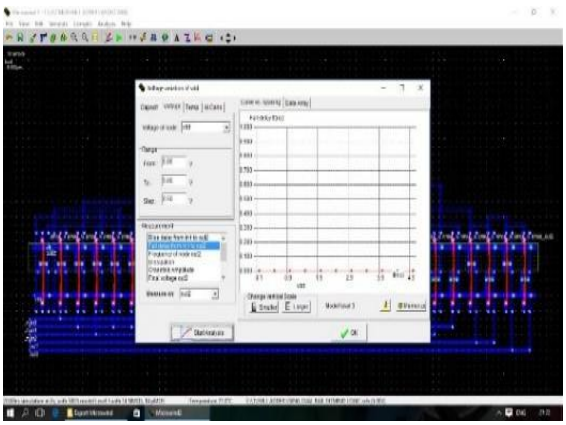

Fig 22 : DPL delay

Comparison Table

Logic	Power dissipation(mw)	Delay(ns)
CMOS	1.108	51.21
TGL	0.752	45.76
PTL	5.432	46.54
Domino Logic	3.920	45.98
DRDL	9.124	46.32
DPL	0.503	45.12

IV. CONCLUSION

The project makes a very significant points that are used while selecting a suitable power and delay reduction techniques. MICROWIND tool is used to design and stimulate the circuits at layout level for different technologies like , Complementary metal oxide semiconductor (CMOS) , Transmission Gate logic (TGL) ,Pass Transistor logic (PTL) , Domino Logic , Dual Rail Domino Logic (DRDL) , Double Pass Transistor logic (DPL) techniques .

Double Pass Transistor logic use only 16 Transistors which is controlled by the output of circuit itself. It achieves the reduction in power and delay compared to other reduction techniques and along with the advantage of not affecting the dynamic power and use of limited area requirements since this technique does not require any additional and monitor circuitry.

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